

Compal Confidential

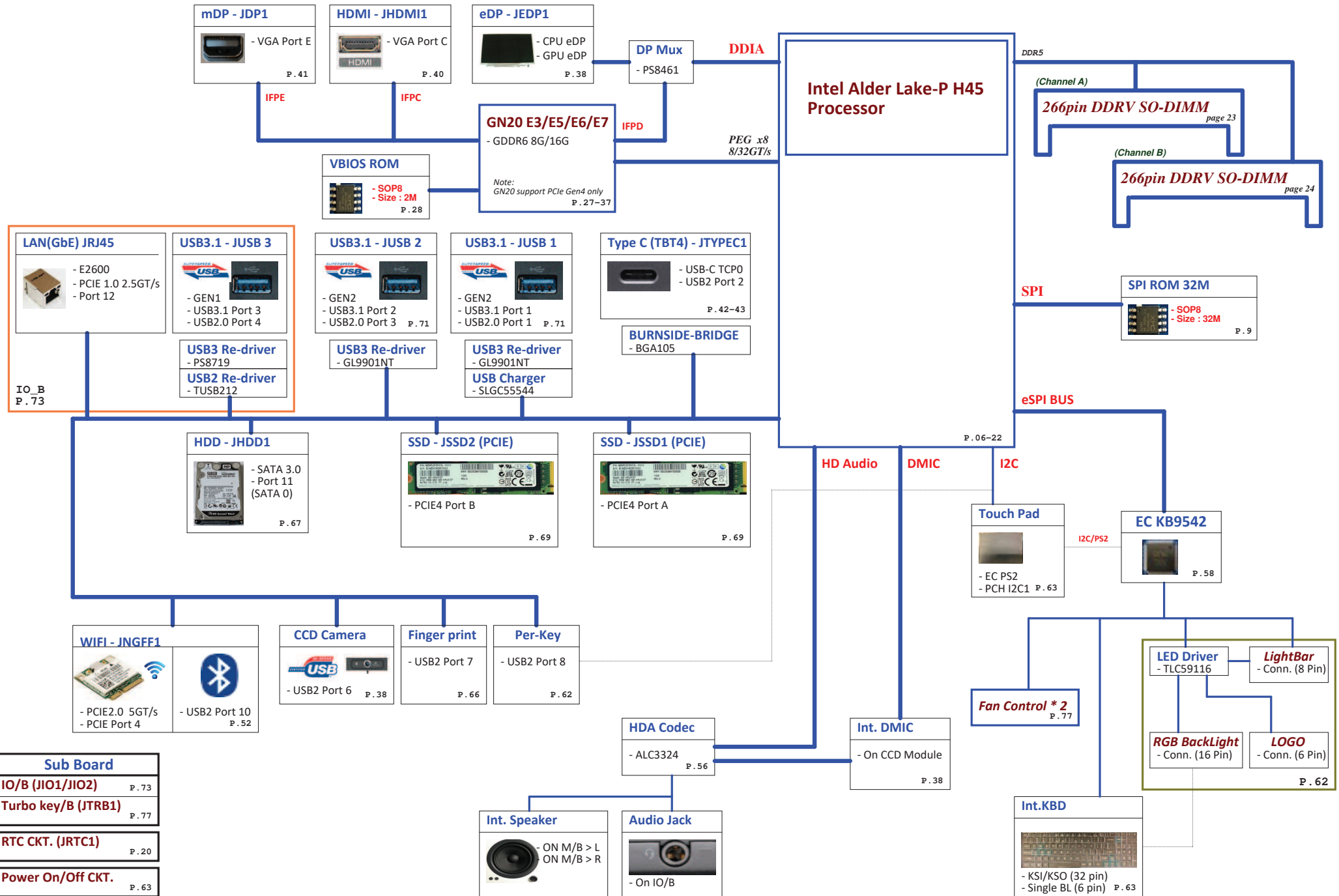
HH53A(60) MB Schematic Document

LA-L992P

Rev : 1B

2021.12.30

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2021/06/07	Deciphered Date	2023/12/31	Title	Cover Sheet
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2021/06/07	Deciphered Date	2023/12/31	Block Diagrams	
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Vcc	3.3V +/- 5%	EC Board ID Table for AD channel			
Ra	100K +/- 1%				
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

SD034120280

SD034150280

SD034200280

SD034270280

SD034330280

SD034430280

SD034560280

SD034750280

SD034100380

SD034130380

SD034160380

SD034200380

SD000001B80

SD000000G280

SD034330380

SD000000WM80

SD034560380

SD000000AL80

*PCB Version
*Key board type

Board ID	PCB Revision
0	50 Rev0.1
1	50 Rev0.2
2	50 Rev1.0
3	
4	50 Rev0.1+RGB
5	50 Rev0.2+RGB
6	50 Rev1.0+RGB
7	
8	60 Rev0.1
9	60 Rev0.2
10	60 Rev1.0
11	60 Rev1.A
12	60 Rev0.1+RGB
13	60 Rev0.2+RGB
14	60 Rev1.0+RGB
15	
16	
17	
18	60 Rev1.A+RGB
19	

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_1	TM-P3393-003 (Touch Pad)			
SOC_SMBCLK	DIMM1	0xA0	0xA1	0xA0
	DIMM2	0xA3	0xA4	0xA3
SOC_SML1	Realtek RTS5452E	0x38		
EC_CK/DA (Port0) (+3VLP)	BQ24800 (Charger IC)	0x12	0001_0010	
	BATTERY PACK	0x16		
EC_CK/DA (Port1) (+3VS)	GN20 E3/E5/E7 (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	0x98	1001_1001b	1001_1000b
	Thermal Sensor (G781)	0x9A	1001_1011b	1001_1010b
EC_CK/DA (Port2)	LED Driver (59116F)	0xC0		
	eDP Mux(P58461E)	0x10-0x2F		
	LightBar	0x5B		
EC_CK/DA (Port3)	Realtek RTS5452E	0x62		0100_0110b
EC_CK/DA (Port5)	KC3810	TBD		

43 Level	Description	BOM Structure
431AUNBOL01	HH53A GN20-E3 QXZR BRL	12VFAN@/CHG@/CMC@/CNVi@/FP@/DA@/DDR4@/DEBUG@/DP@/GLITCH@/GN20E@/HDD@/KC3810@/LB@/LED14P@/LOGOBL@/NGSYNC@/OVRM@/PERKEY@/TMS@/TypeC@/VGA@/X4E@/2012@/GN20E3@/15ES2@/EVT@/SLGC55544@/X76SAM6G@/X76UPIGEN2/COST@
431AUNBOL02	HH53A GN20-E3 QXZR B3L	
431AUNBOL03	HH53A GN20-E5 QYQZ BRL	
431AUNBOL04	HH53A GN20-E5 QYQZ B3L	
431AUNBOL05	HH53A GN20-E7 QXZH BRL	

V : Must V : Options

Item (X43 / X76)	BOM Structure	Item (X43 / X76)	BOM Structure
Unpop	@	USB Chager	CHG@ V
Connector	CONN@	XDP	CMC@ V
PCB	DAZ@ V	KC3810	KC3810@ V
ADL-P		Intel CNVi	CNVi@ V
		FOR UART debug	UART@ V
		EC debug	DEBUG@ V
FJ8071504786411 Q07K	i9SUPQS@ V	Finger Print	FP@ V
FJ8071504785804 SRLCY L0	i7MP@ V	KB LED driver	LED14P@ V
FJ8071504786106 SRLD1 L0	i5MP@ V	Thermal sensor	TMS@ V
GN20E GPU	GN20E@ V	GLITCH	GLITCH@ V
GN20-E3-A1	GN20E3@ V	CMC	CMC@ V
GN20-E5-A1	GN20E5@ V	Power PRIM Design	PREM@ V
		TypeC Port	TypeC@ V
GN20-E7-A1	GN20E7@ V	HDD	HDD@ V
dGPU circuit	VGA@ V	Lightbar	LB@ V
GPU OVRM	OVRM@ V	Acer Logo backlight	LOGOBL@ V
mDP	DP@ V	DDR4 strap	DDR4@ V
		DDR5 strap	DDR5@ V
		CW3046	CW3046@ V
		SLGC55544	SLGC55544@ V
		XTAL Package 2012	2012@ V
		XTAL Package 3215	3215@ V
		DD5 Support	GSYNC@ V
		DDS Not Support	NGSYNC@ V
		12V FAN	12VFAN@ V

Item(X4E)un-pop	BOM Structure
EMI require reserve	XEMI@
EMC require reserve	XEMC@
ESD require reserve	XESD@
RF require reserve	@RF@

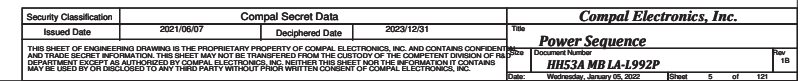
EC Board ID	BOM Structure
HH53A 0.1 without RGB	R01@ V
HH53A 0.1 with RGB	R01RGB@ V
HH53A 0.2 without RGB	R02@
HH53A 0.2 with RGB	R02RGB@

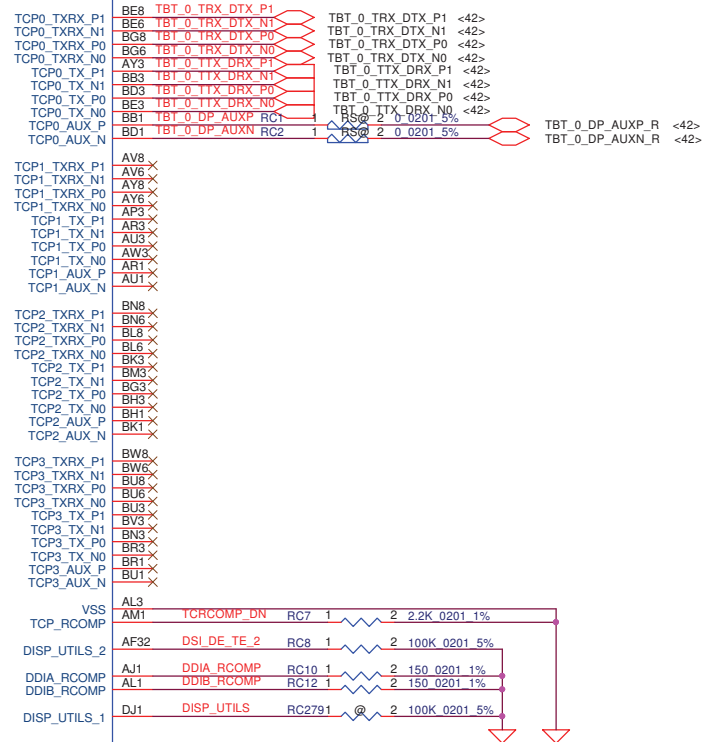
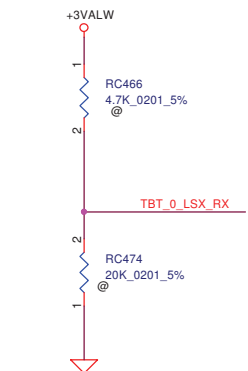
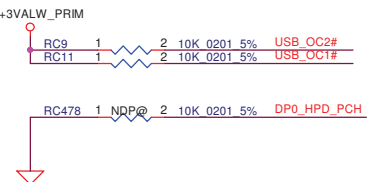
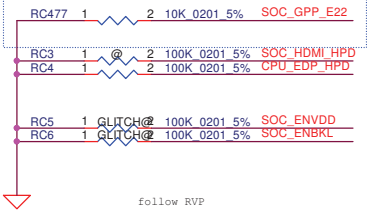
Item (X4E) pop	BOM Structure
EMI requirement	EMI@ V
EMC requirement	EMC@ V
ESD requirement	ESD@ V
RF require reserve	RF@ V
FP EMC requirement	FPEMC@ V
FP ESD requirement	FPESD@ V
TBT ESD requirement	BL_ESD@ V
TBT EMC requirement	BL EMC@ V
X4EAUNBOL01	EMC M/B 60 LAL992

Item (X76)	BOM Structure
OVRM-uPI Gen2	X76UPIGEN2@
OVRM-ON Gen2	X76ONGEN2@
OVRM-uPI Gen1	X76UPIGEN1@
OVRM-ON Gen1	X76ONGEN1@
VRAM-SAMSUNG 6G	X76SAM6G@
VRAM-HYNIX 6G	X76HYN6G@
VRAM-Mircon 6G	X76MIR6G@
VRAM-SAMSUNG 8G	X76SAM8G@
VRAM-HYNIX 8G	X76HYN8G@
VRAM-Mircon 8G	X76MIR8G@

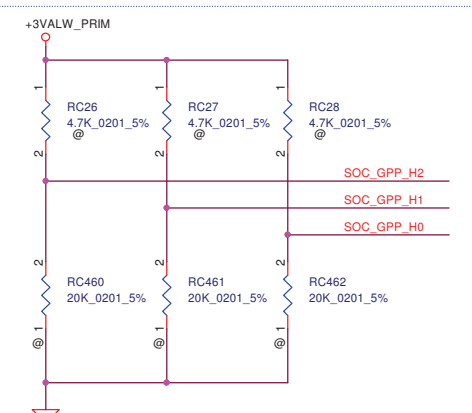
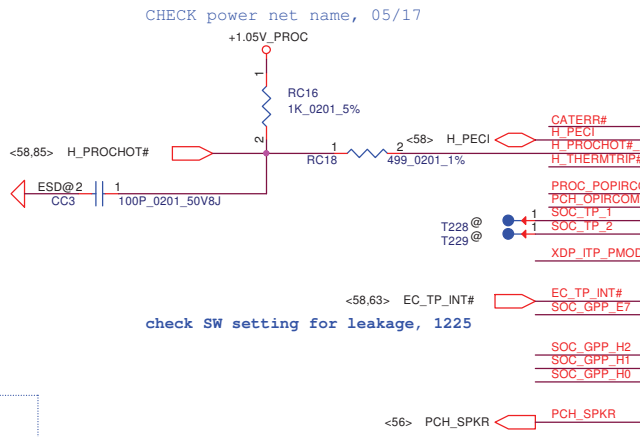
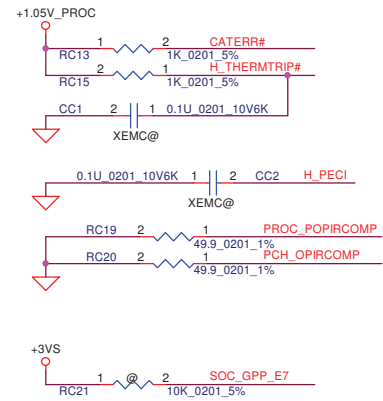
X76952BOL05 - UPI Gen2 OVRM
X76952BOL06 - ON Gen2 OVRM
X76952BOL11 - UPI Gen1 OVRM
X76952BOL12 - ON Gen1 OVRM
X76952BOL01 - SAMSUNG 6G
X76952BOL02 - HYNIX 6G
X76952BOL13 - Mircon 6G
X76952BOL03 - SAMSUNG 8G
X76952BOL04 - HYNIX 8G
X76952BOL09 - Mircon 8G

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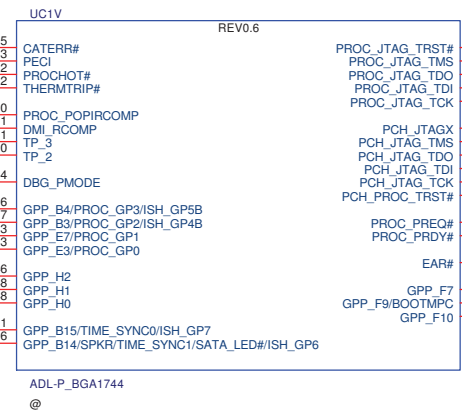
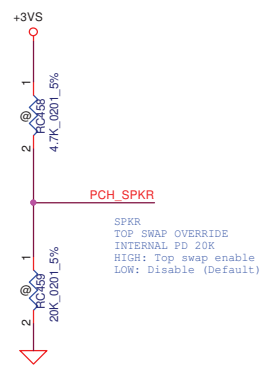
SOC_GPP_H2
BOOT STRAP3 - BIT3
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_GPP_H1
BOOT STRAP1 - BIT2
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

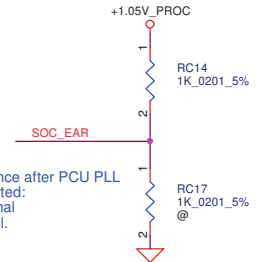
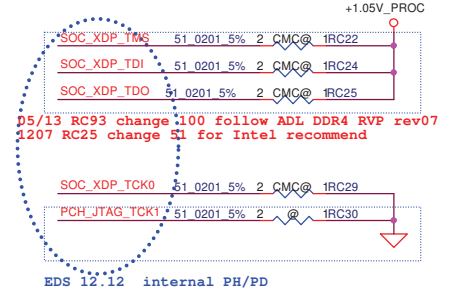
SOC_GPP_H0
BOOT STRAP1 - BIT1
This is bit 1 of a total of 4-bit encoded pin straps for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
INTERNAL PD 20K

SOC_WWAN_RST# (No used)
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
INTERNAL PD 20K

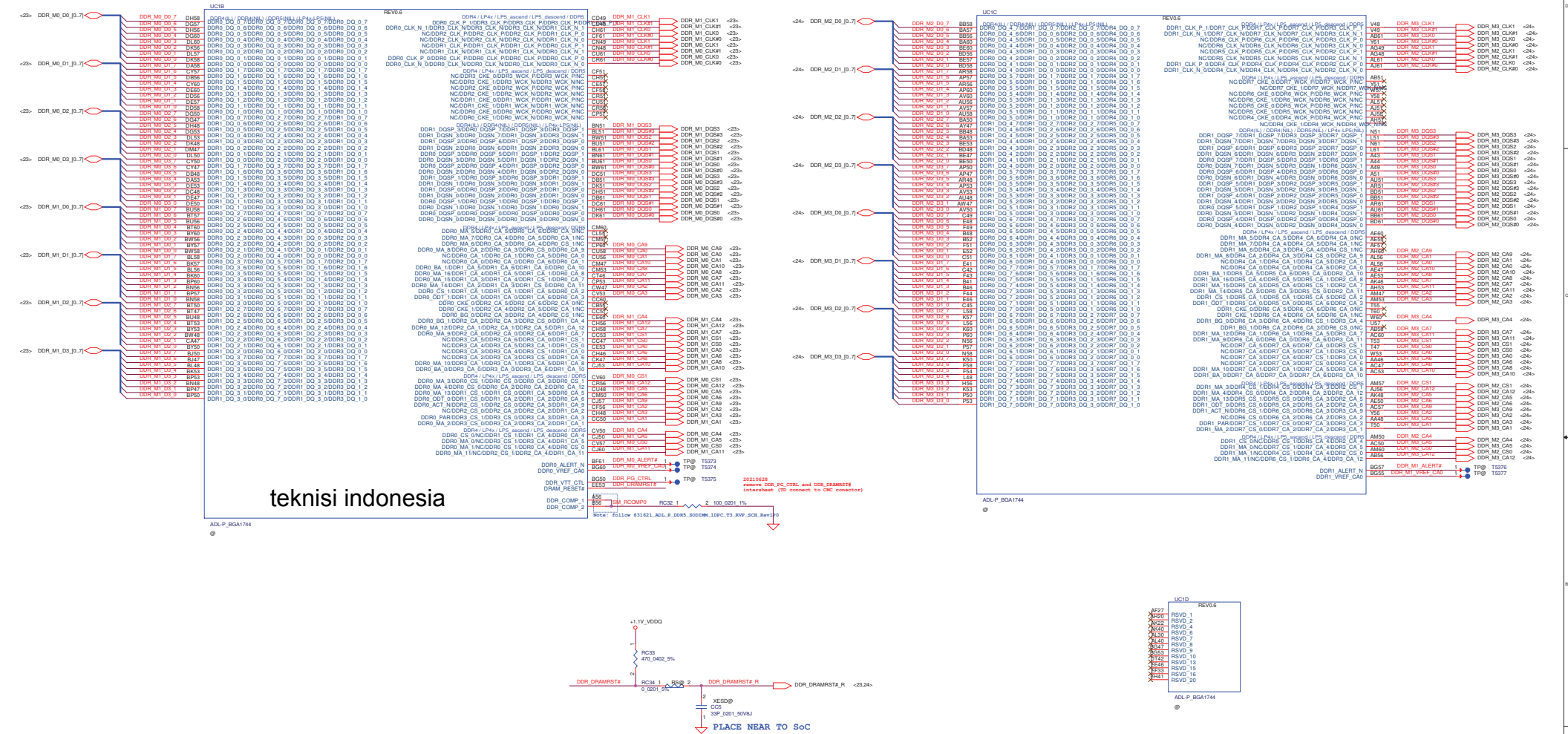
Strap Pin



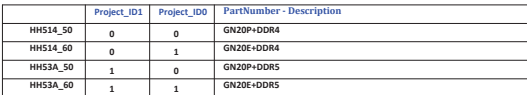
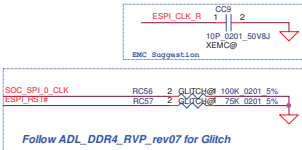
- R6 SOC_XDP_TRST#
- U8 SOC_XDP_TMS
- AA6 SOC_XDP_TDO
- W8 SOC_XDP_TDI
- N6 SOC_XDP_TCK
- N8 SOC_XDP_TCK0
- U6 SOC_XDP_TMS
- AA8 SOC_XDP_TDO
- W6 SOC_XDP_TDI
- FB6 PCH_JTAG_TCK1
- R8 SOC_XDP_TRST#
- L6 XDP_FREQ#
- L8 XDP_PRDY#
- AF25 SOC_EAR
- EN28
- ET28
- EF28



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								Size	Document Number		Rev
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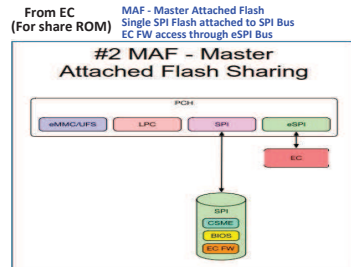


tekni indonesia

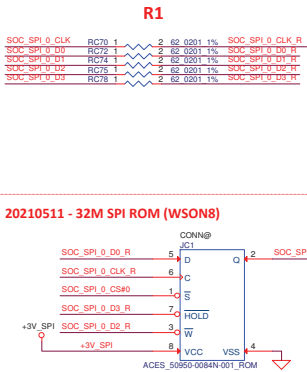
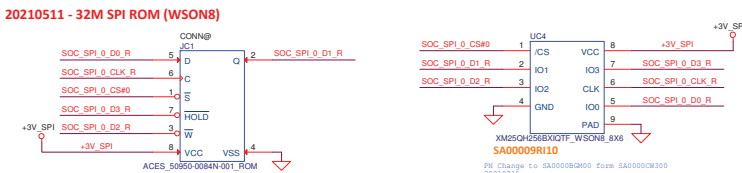


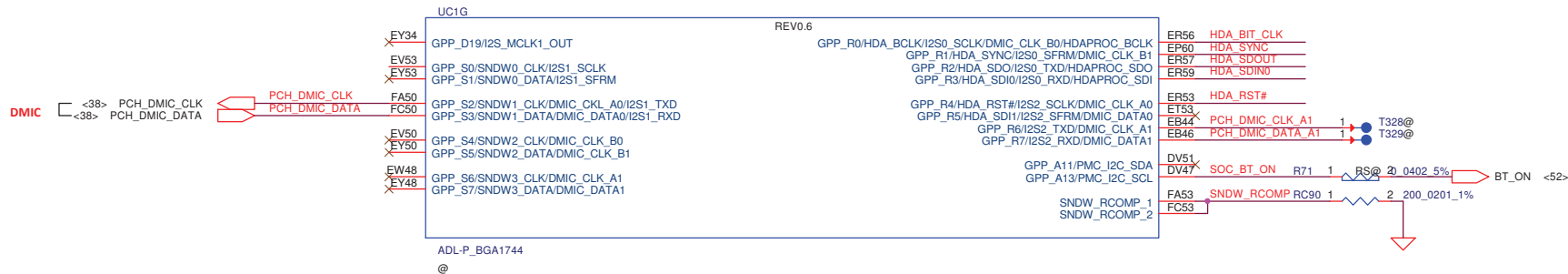
*** SPI0 3 load topology:
R1 is required 15 ohm \pm 10% for 1.8V, 33 ohm \pm 5% for 3.3V.
R2 is required 10 ohm for 1.8V and 3.3V.
It is an optional to have R2 on the channel. It can be removed to reduce BOM cost

*** CS# does not need series resistor



20210528 remove TPM

20210604
remove 16M SPI ROM

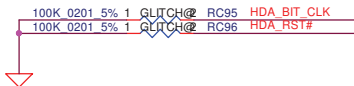


HDA for AUDIO

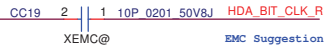
20200819

- Remove RC180 BOM config., must pop of PDG.

<56>	HDA_SDOUT_R	HDA_SDOUT_R	RC31	1	2	33	0201	5%	HDA_SDOUT
<56>	HDA_BIT_CLK_R	HDA_BIT_CLK_R	RC32	1	2	33	0201	5%	HDA_BIT_CLK
<56>	HDA_SYNC_R	HDA_SYNC_R	RC93	1	2	33	0201	5%	HDA_SYNC
<56>	HDA_RST#_R	HDA_RST#_R	RC94	1	2	33	0201	5%	HDA_RST#
<56>	HDA_SDINO	HDA_SDINO							

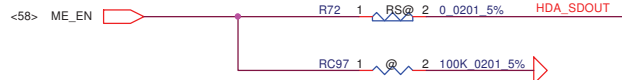


Follow
627205_ADL P_PDG for Glitch



To Enable ME Override

HDA_SDOUT
FLASH_DESCRIPTOR SECURITY OVERRIDE
INTERNAL PD 20K
HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)

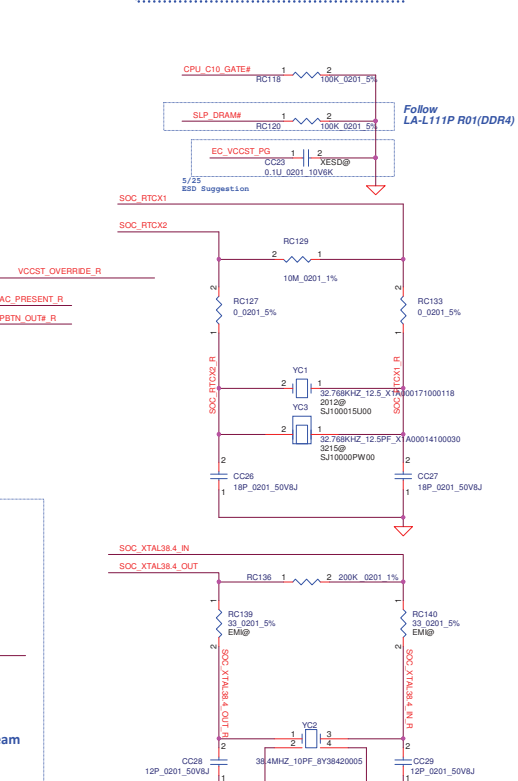
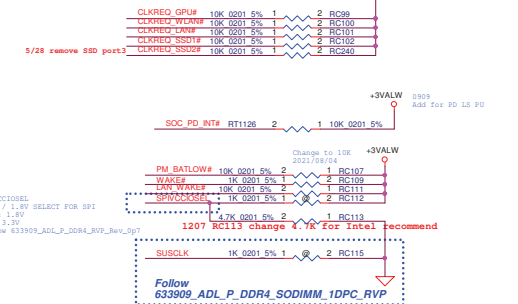
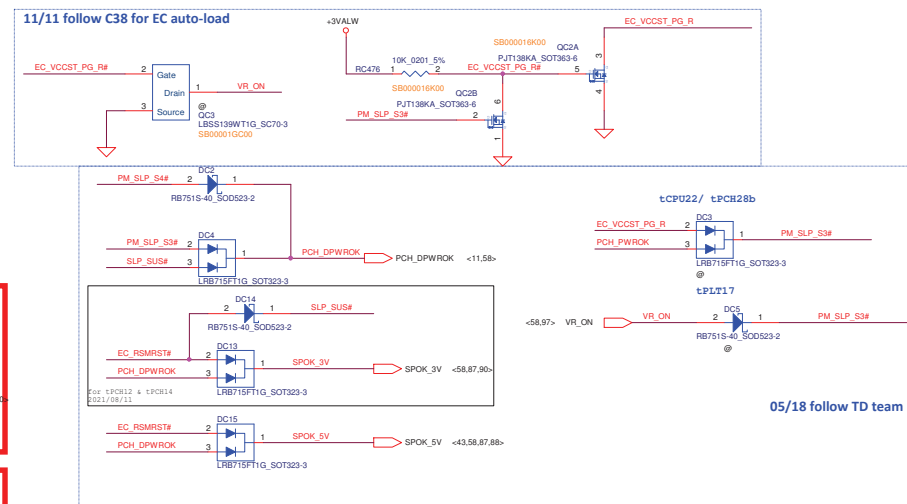
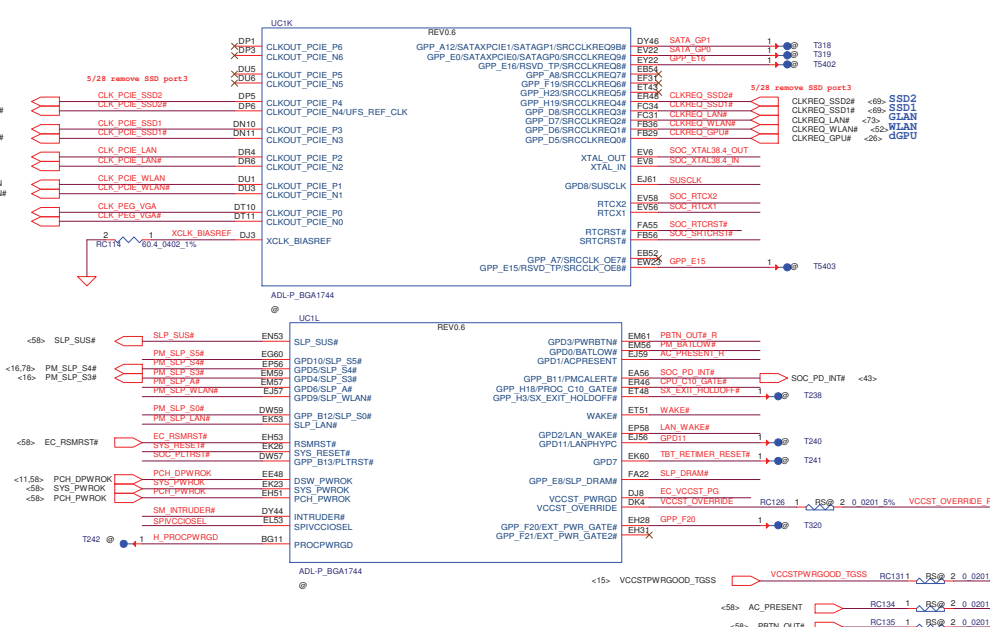
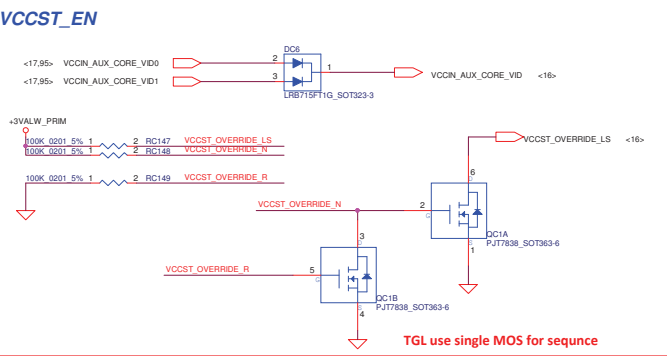
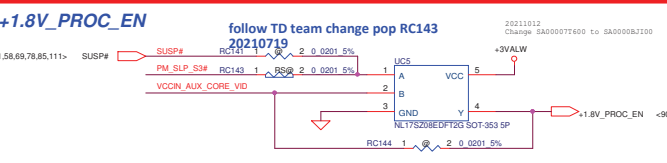
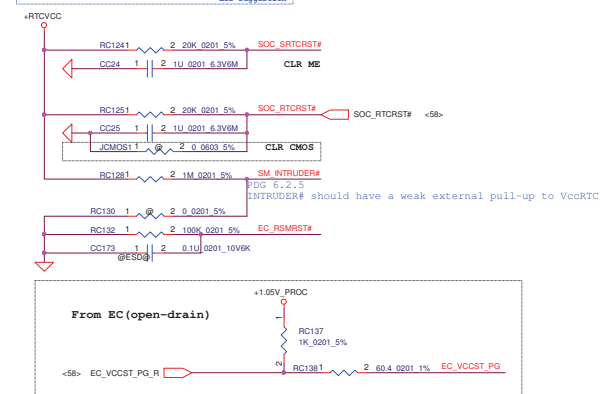
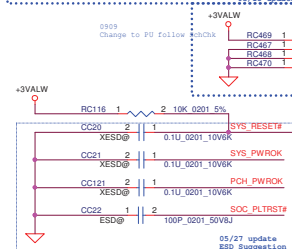
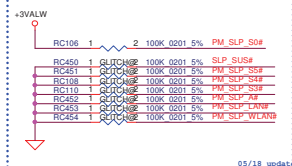


572631_ICL_PCH_LP_EDS_Vol_1_Rev_0p7
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO

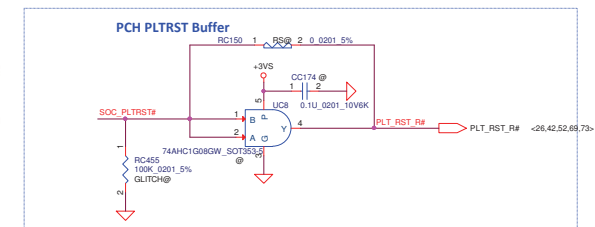
HDA_SYNC	CC12	@RF@1	2	22P	0201	25V8
HDA_BIT_CLK	CC13	@RF@1	2	22P	0201	25V8
HDA_SDOUT	CC14	@RF@1	2	22P	0201	25V8
HDA_SDINO	CC15	@RF@1	2	22P	0201	25V8
HDA_RST#	CC16	@RF@1	2	22P	0201	25V8
PCH_DMIC_CLK	CC17	@RF@1	2	22P	0201	25V8
PCH_DMIC_DATA	CC18	@RF@1	2	22P	0201	25V8

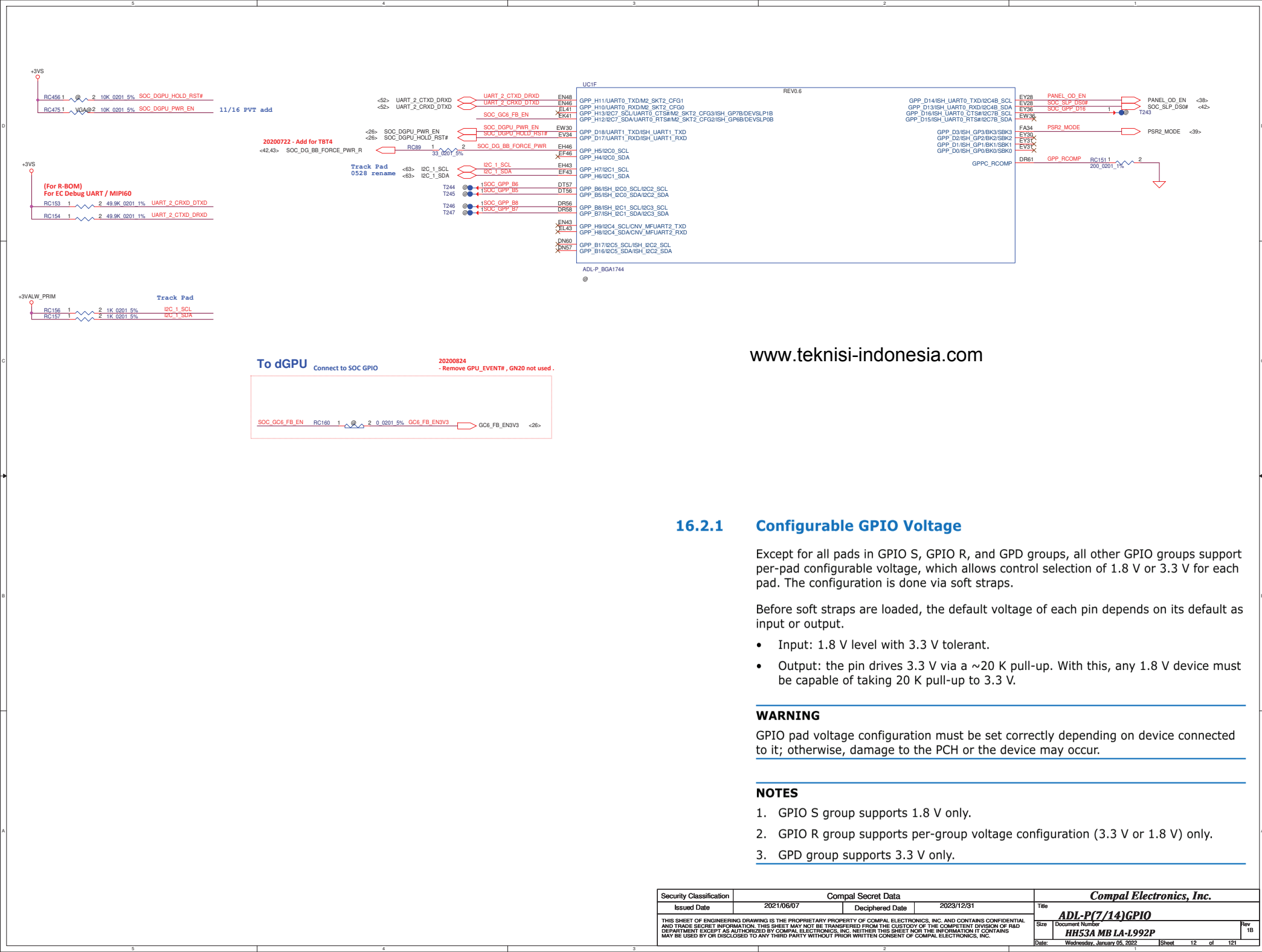
Close SOC

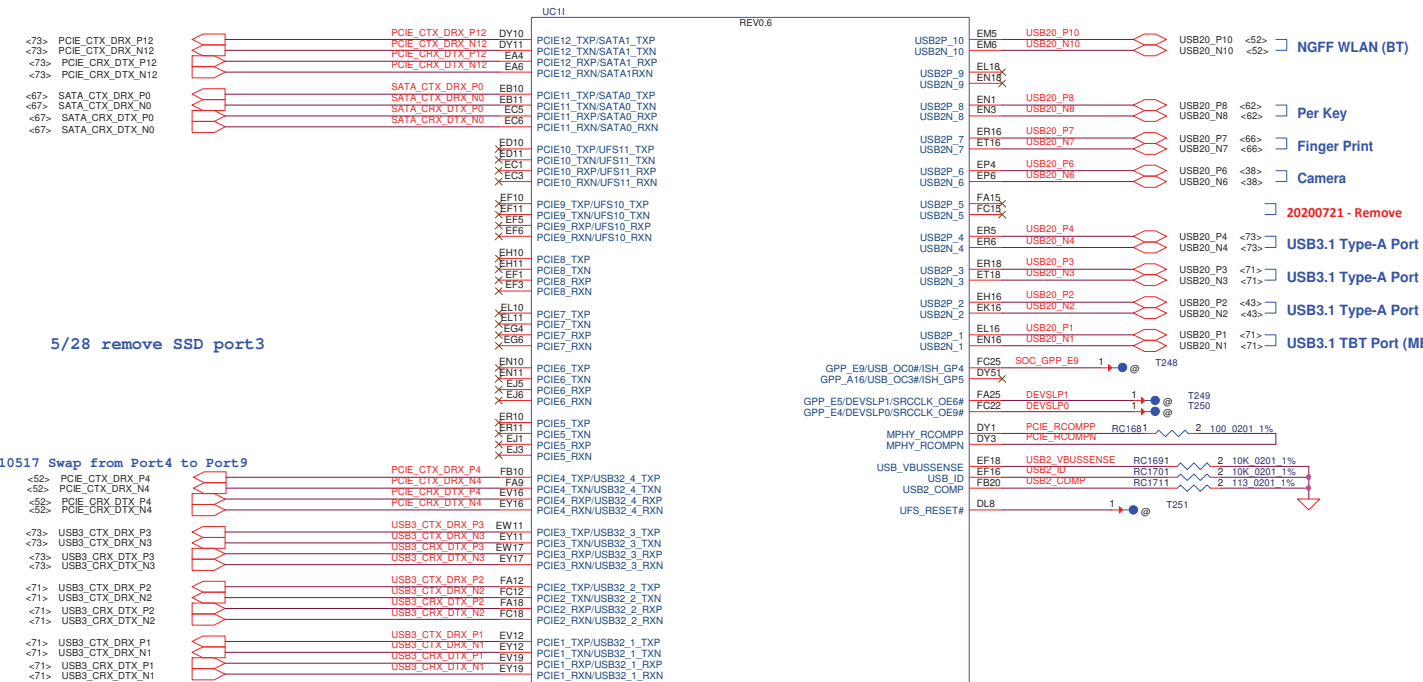
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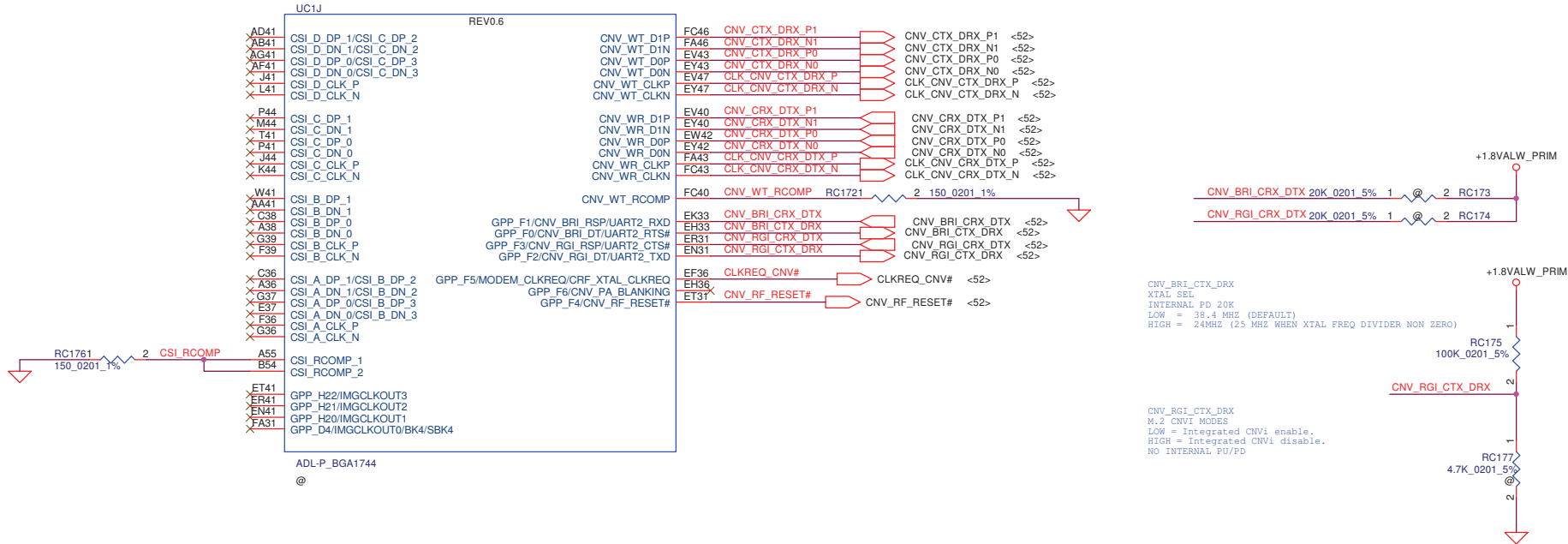
Signal Name	Type	SSC Capable	Description
<ul style="list-style-type: none"> CLKOUT_PCIE_P [6:0] CLKOUT_PCIE_N [6:0] 	0	Yes	PCI Express® Clock Output: Serial Reference 100 MHz PCIe® specification compliant differential output clocks to PCIe® devices <ul style="list-style-type: none"> CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe® Gen1, Gen2, and Gen3 support CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe® Gen4 support



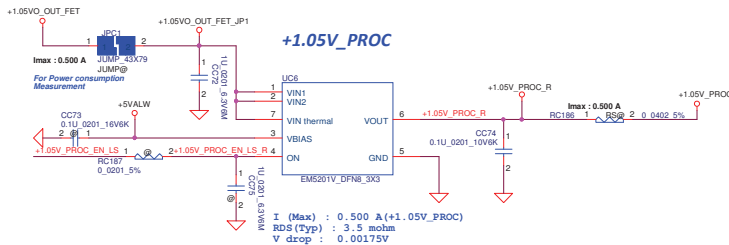
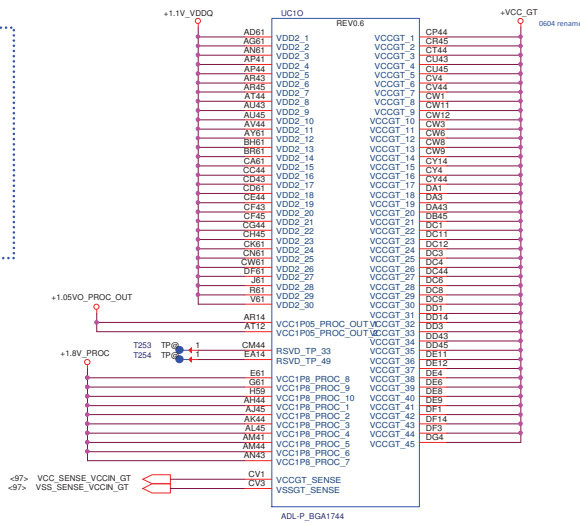
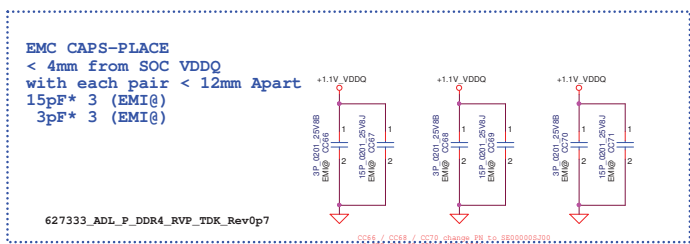




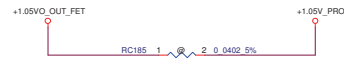
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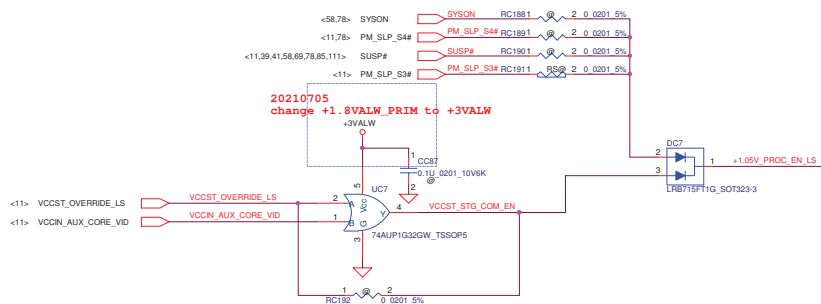
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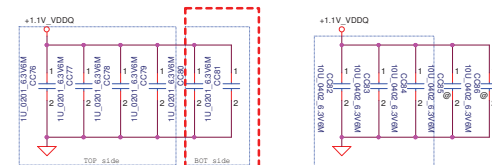
NOTE

Sideband signals(PECI,THERMTRIP,PROCHOT,VCCST_PWRGD,SVID) should be connected to **VCC1P05_PROC** rail when there is Power Gate or to **VCC1P05_OUT_FET** (which should be shorted to VCC1P05_OUT_FET)rail when there is no Power Gate.

+1.05V_PROC Enable

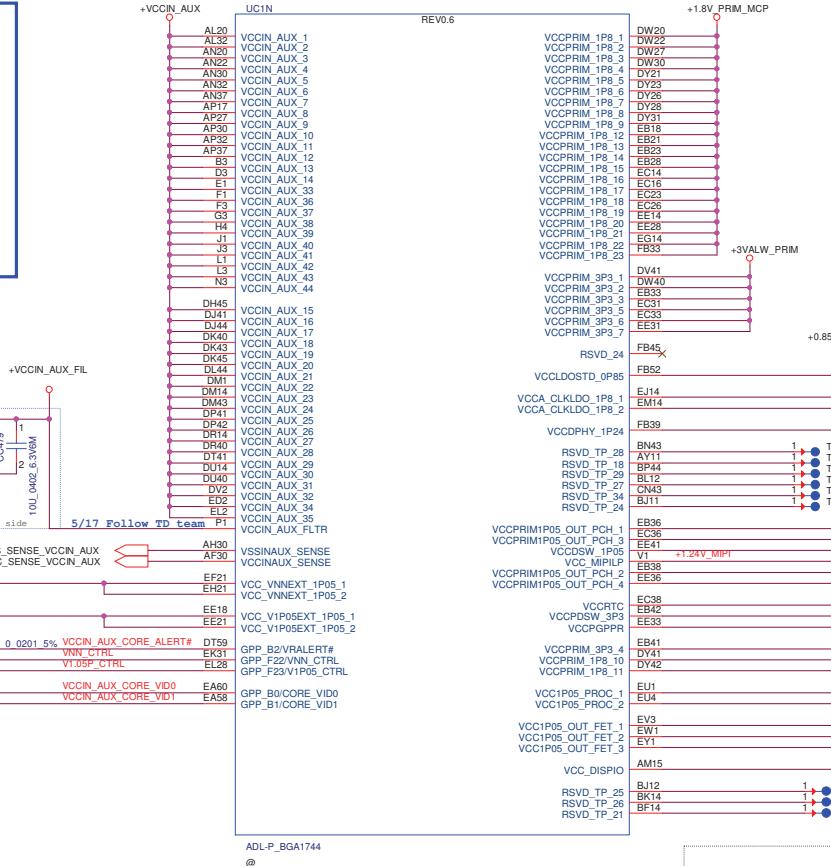
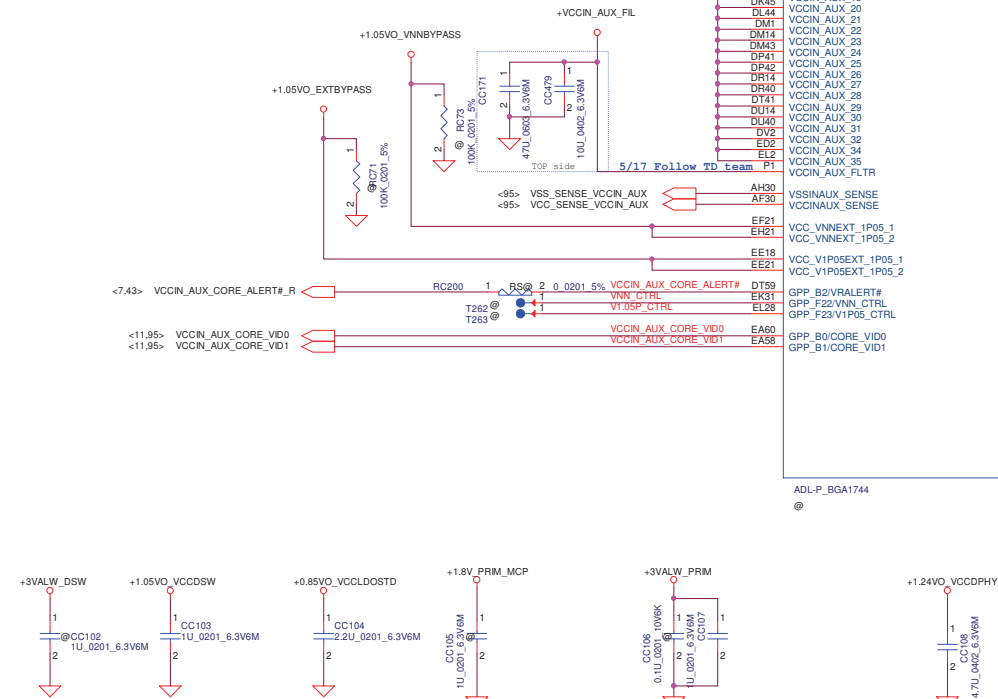
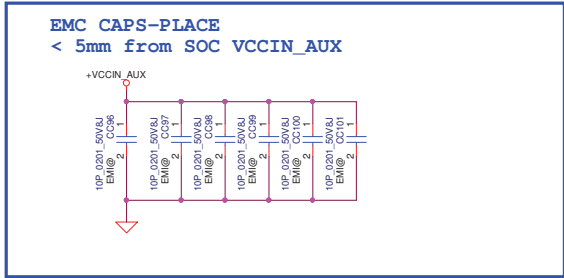
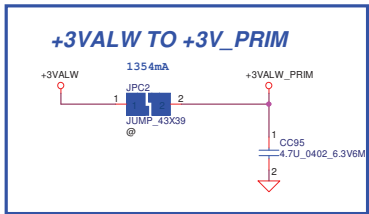


1uF* 6
 10uF * 3
 uF * 2
 Layout Follow 627205_ADL_P_PDQ_Rev0p7



TO team DDB circuit in 100, 0402 (8)

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Note: VCCPGPPR follow HDA interface
1.2.2.6 VCCPGPPR

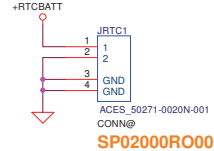
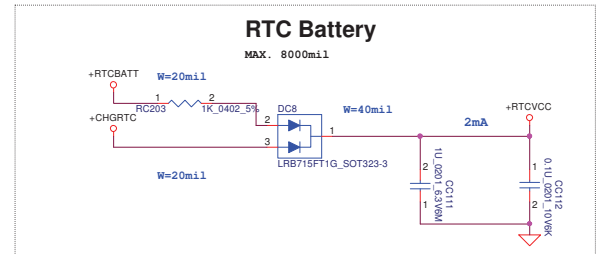
Description: Intel HD Audio Supply. Can operate at 3.3V or 1.8V

Settings

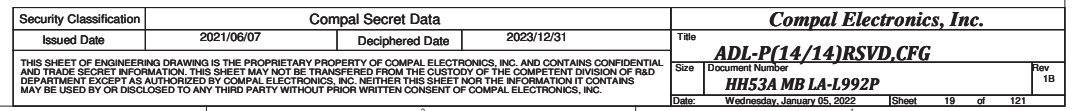
Table 818. Reference Layout Design

Index	Design Note	Reference Design
1	VCCPGPPR can be merged directly to either VCCPRIM_3P3 or VCCPRIM_1P8 power plane depending on the operating voltage. Required immediate ground reference for VCCPGPPR power plane.	
2	If operating at 3.3V: Merge VCCPGPPR PTH with VCCPRIM_3P3 plane.	GPFR_1
3	If operating at 1.8V: Extend VCCPGPPR to merge with VCCPRIM_1P8 plane.	GPFR_2

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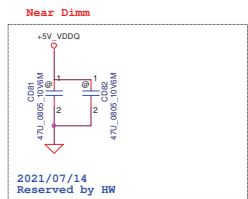
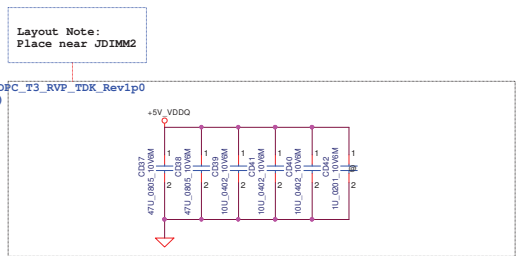
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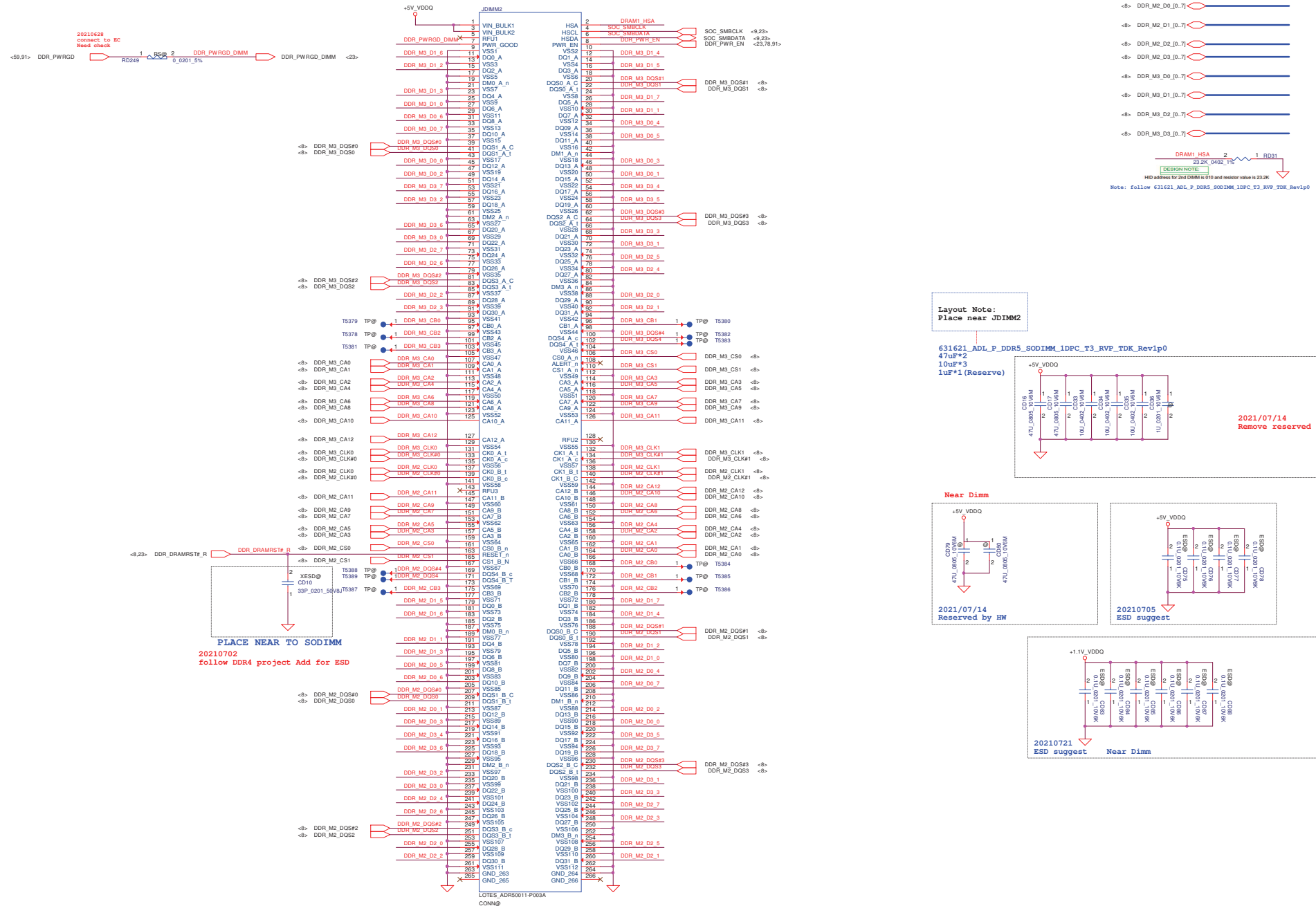
Non-Interleaved Memory



Part Number:SP012010053
Part Value:LOTES_ADR50012-P003A

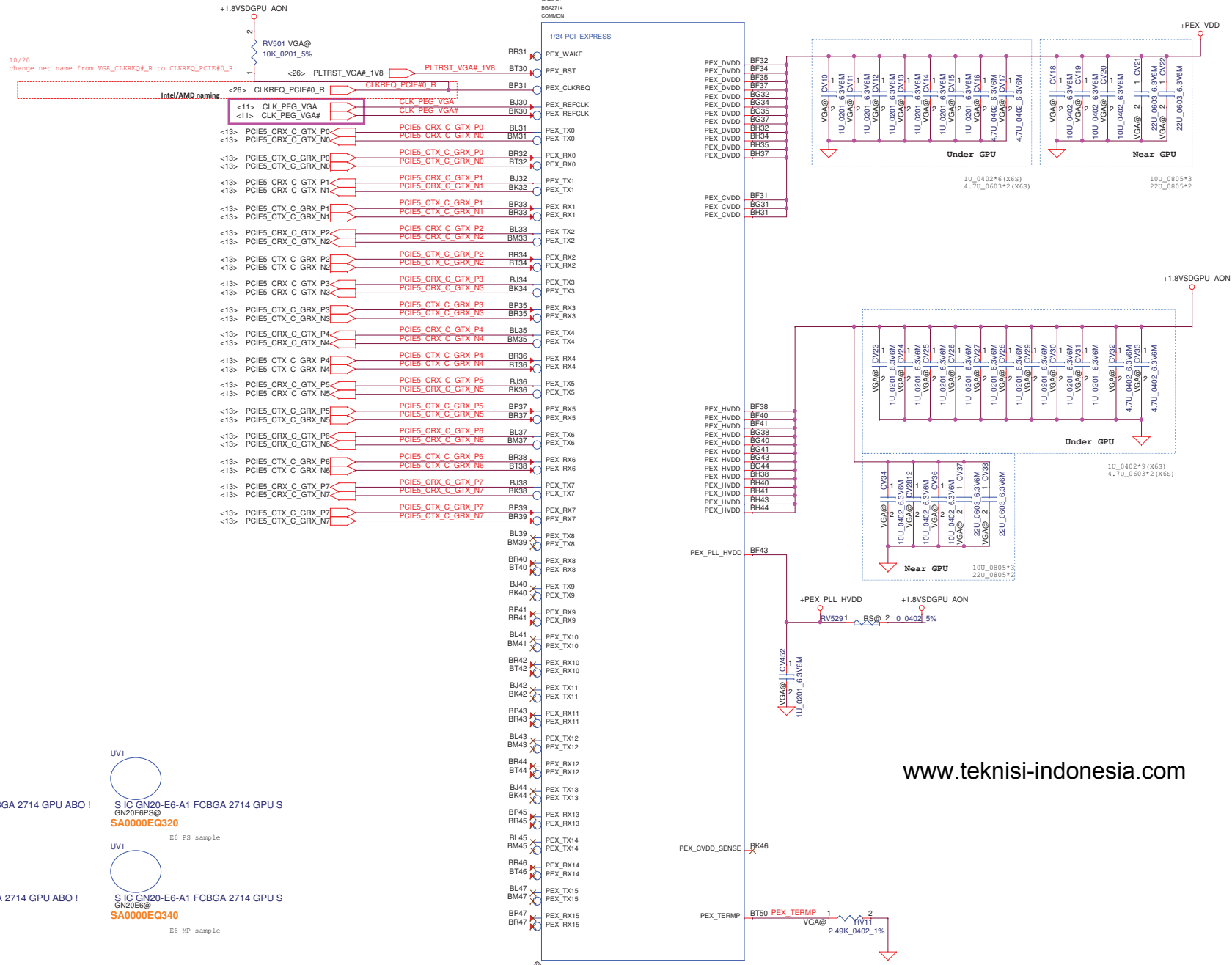
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Non-Interleaved Memory



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AMD FP6 only support x8



UV1
S IC GN20-E3-A1 FCBGA 2714 GPU ABO I
GN20E3@
SA0000E1930

UV1
S IC GN20-E6-A1 FCBGA 2714 GPU S
GN20E6@
SA0000EQ320

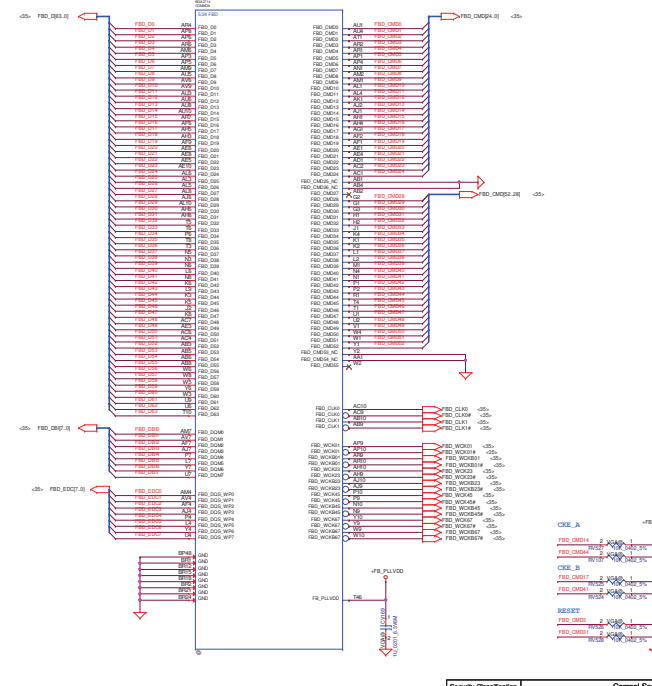
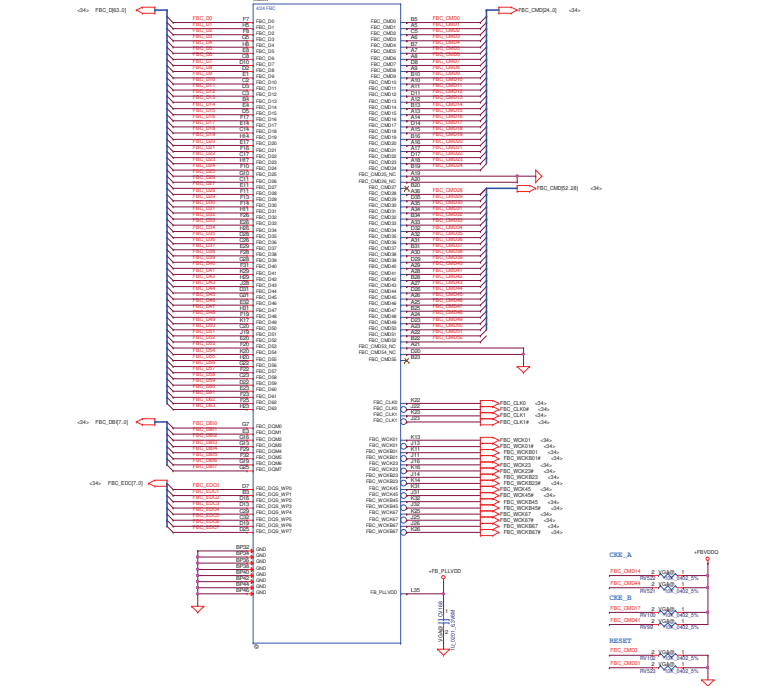
UV1
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GN20E5@
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UV1
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SA0000EQ340

UV1
S IC GN20-E7-A1 BGA 2714 GPU ABO I
GN20E7@
SA0000DUM20

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Table with 2 columns: Strap Pins, Functions Selected by This Strapping. Rows include various strap pins like STRAP0, STRAP1, STRAP2, STRAP3, STRAP4, STRAP5 and their functions like SMB_ALT_ADDR, DEVID_SEL, FIDIE_CFG, VGA_DEVICE.

Table with 2 columns: Memory Density, Vendor, Manufacture part Number, Die Revision, Strap, Strap2, Strap1, Strap0, 2N20-E7, 2N20-E5, 2N20-E3, 2N20-E1, 2N20-E3, 2N20-E5.

Table 5. GN20-E3 GDDR6 Recommended Memories. Table with 2 columns: Allowed Memory Configuration, Vendor, Manufacture Part Number, Die Revision, Strap, Memory Speed Grade, Data Code Alert, Qual. Plan, Status, Supported GPU Memory.

Table 6. GN20-E5 GDDR6 Recommended Memories. Table with 2 columns: Allowed Memory Configuration, Vendor, Manufacture Part Number, Die Revision, Strap, Memory Speed Grade, Data Code Alert, Qual. Plan, Status, Supported GPU Memory.

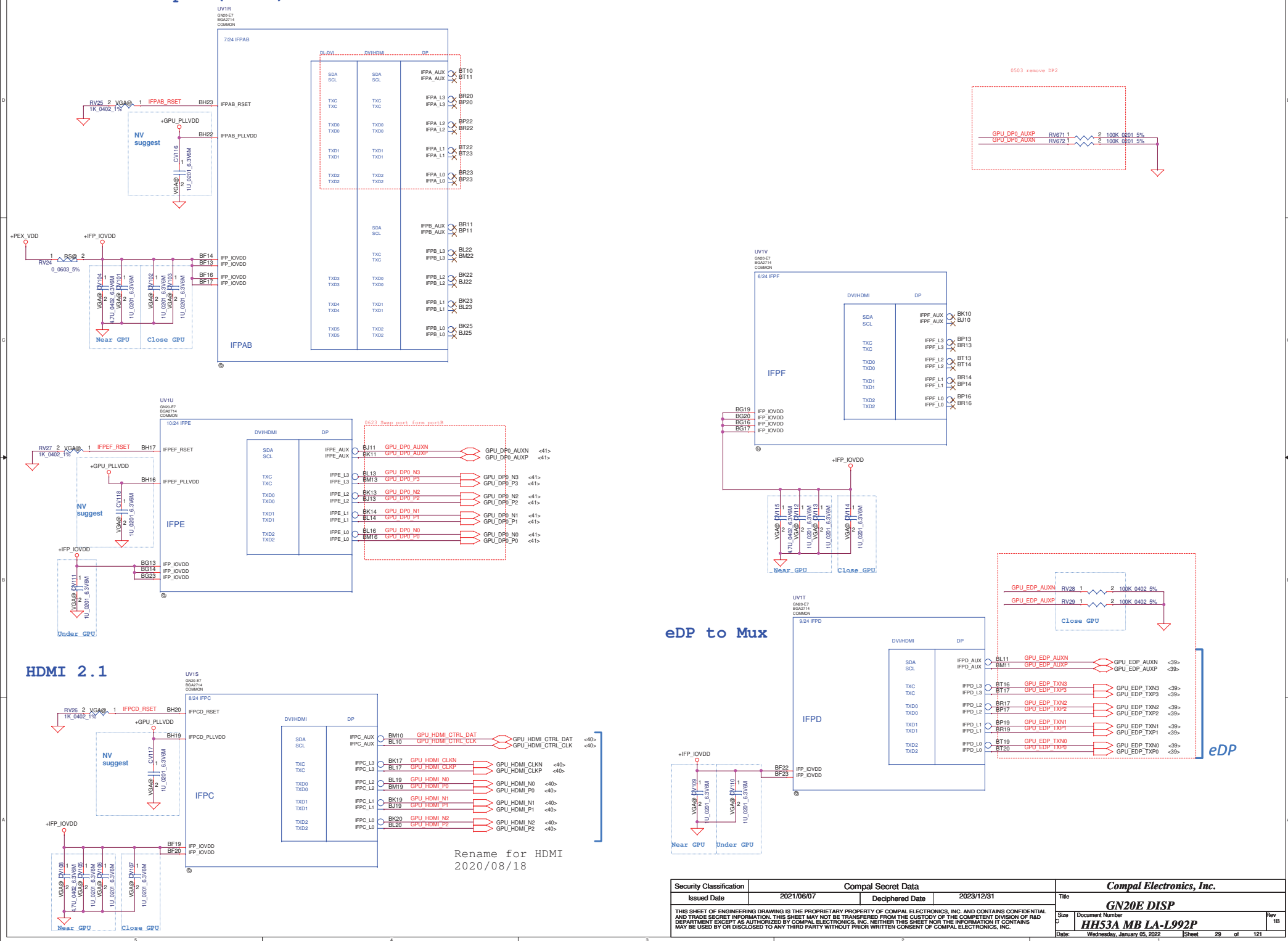
Table with 2 columns: X76VSAM@, X76VSM@, X76VSM@, X76VSM@, X76VSM@, X76VSM@. Rows include various memory configurations and their supported GPU memory.

Table with 2 columns: X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@. Rows include various memory configurations and their supported GPU memory.

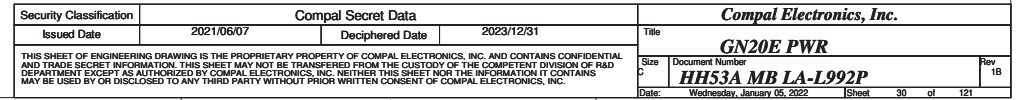
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Table with 2 columns: X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@, X76VHYNADIE@. Rows include various memory configurations and their supported GPU memory.

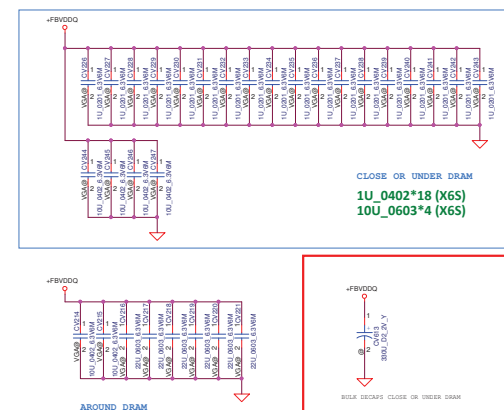
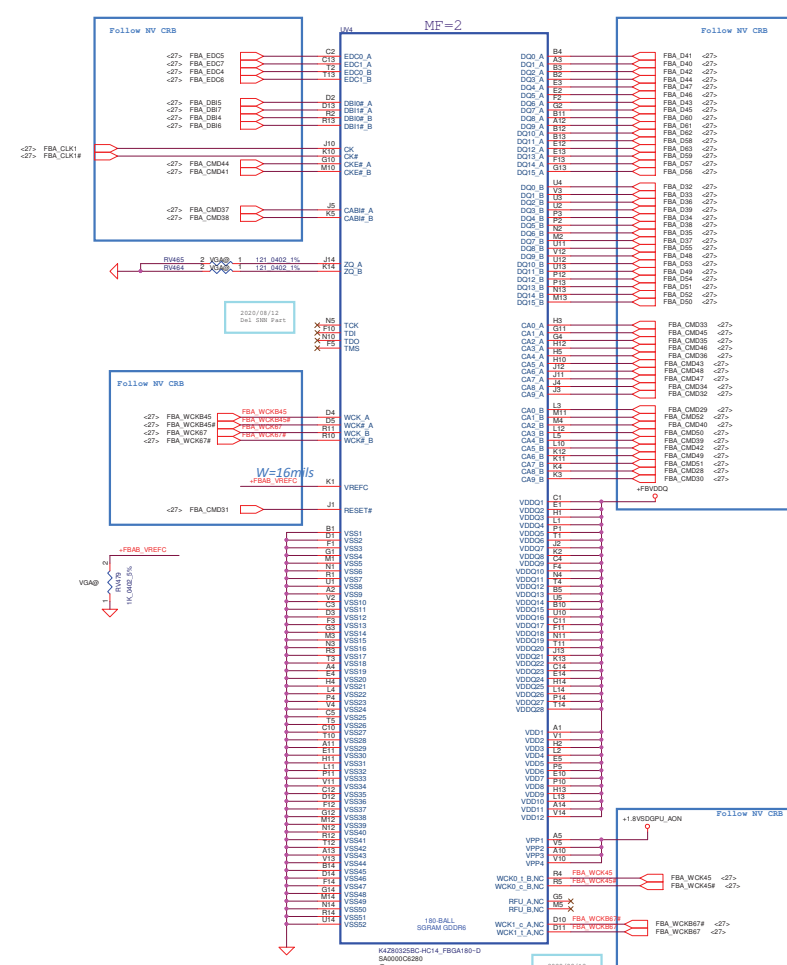
HDMI 2.1



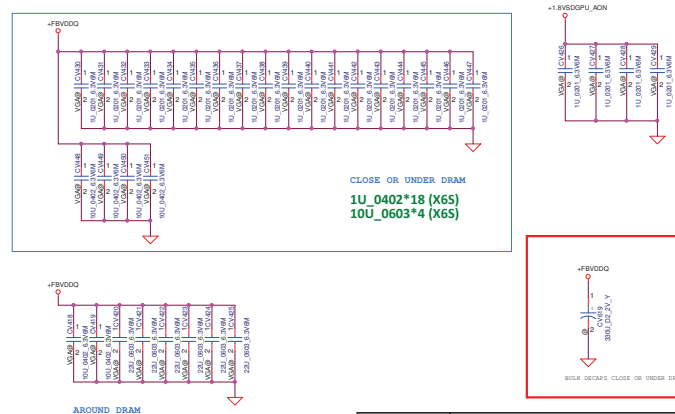
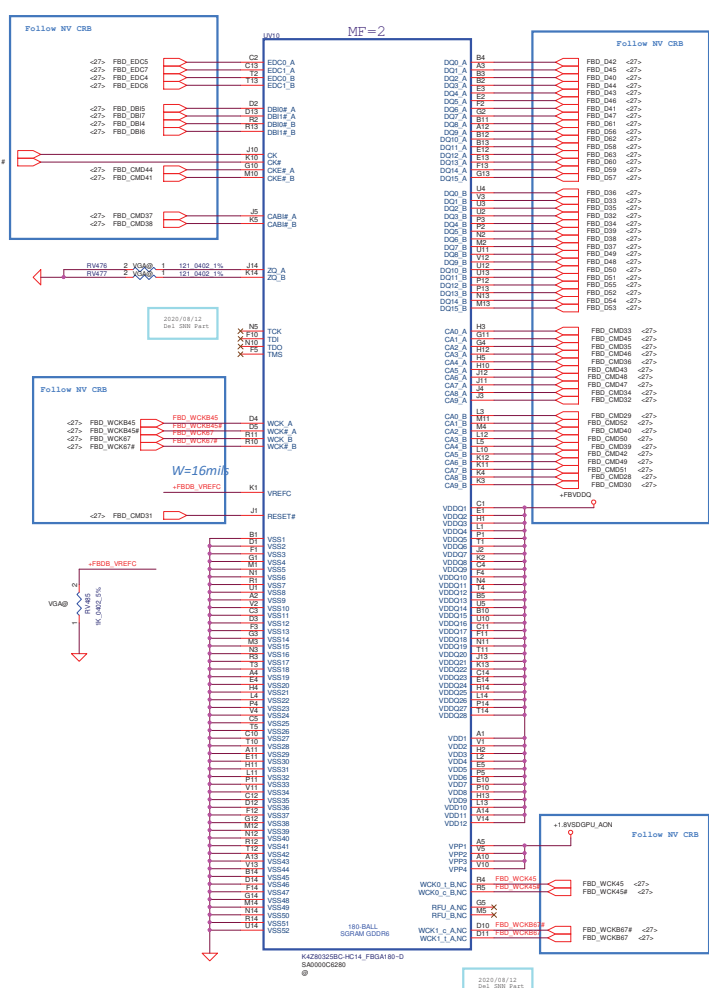
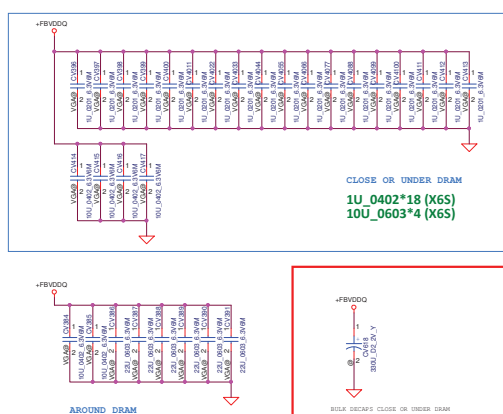
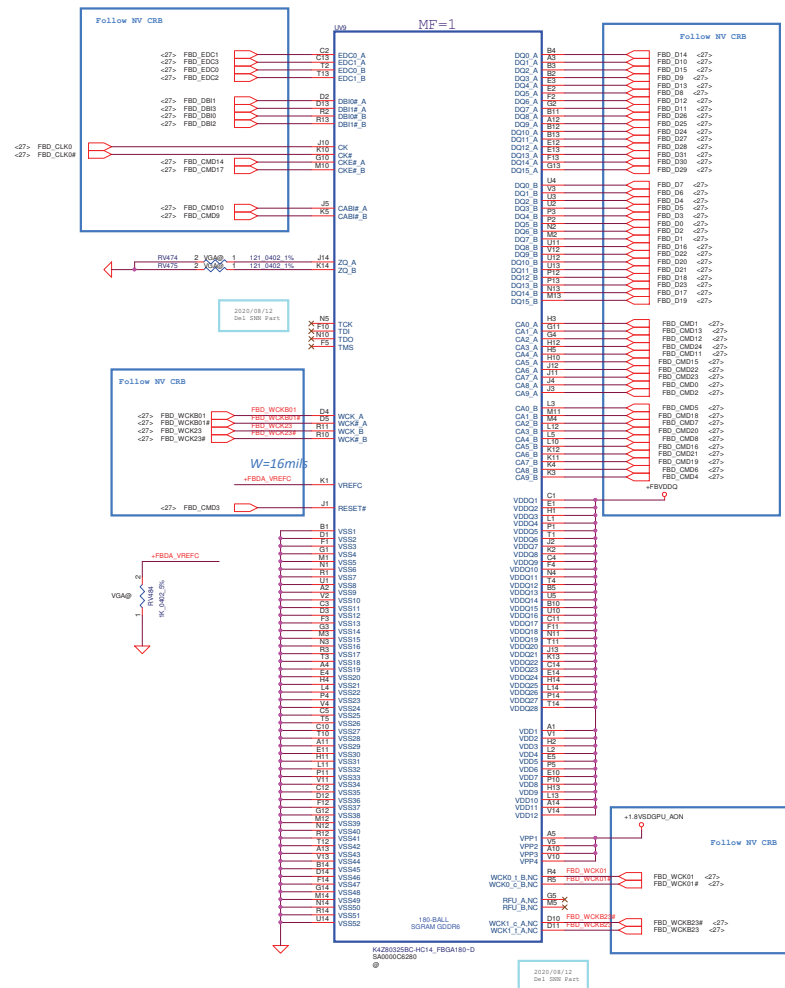
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GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FbX_CND0	Bytes 0,1: CA0_A Bytes 2,3: CA0_B	FbX_CND16	Bytes 4,5: CA0_A Bytes 6,7: CA0_B
FbX_CND1	Bytes 0,1: CA1_A Bytes 2,3: CA1_B	FbX_CND17	Bytes 4,5: CA1_A Bytes 6,7: CA1_B
FbX_CND2	Bytes 0,1: CA2_A Bytes 2,3: CA2_B	FbX_CND18	Bytes 4,5: CA2_A Bytes 6,7: CA2_B
FbX_CND3	Bytes 0,1: CA3_A Bytes 2,3: CA3_B	FbX_CND19	Bytes 4,5: CA3_A Bytes 6,7: CA3_B
FbX_CND4	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FbX_CND20	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FbX_CND5	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FbX_CND21	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FbX_CND6	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FbX_CND22	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FbX_CND7	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FbX_CND23	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FbX_CND8	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FbX_CND24	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FbX_CND9	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FbX_CND25	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FbX_CND10	Bytes 0,1: CA10_A Bytes 2,3: CA10_B	FbX_CND26	Bytes 4,5: CA10_A Bytes 6,7: CA10_B
FbX_CND11	Bytes 0,1: CA11_A Bytes 2,3: CA11_B	FbX_CND27	Bytes 4,5: CA11_A Bytes 6,7: CA11_B
FbX_CND12	Bytes 0,1: CA12_A Bytes 2,3: CA12_B	FbX_CND28	Bytes 4,5: CA12_A Bytes 6,7: CA12_B
FbX_CND13	Bytes 0,1: CA13_A Bytes 2,3: CA13_B	FbX_CND29	Bytes 4,5: CA13_A Bytes 6,7: CA13_B

Notes:
 1. GPU debug pins; not connected to DRAM.
 2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
 3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

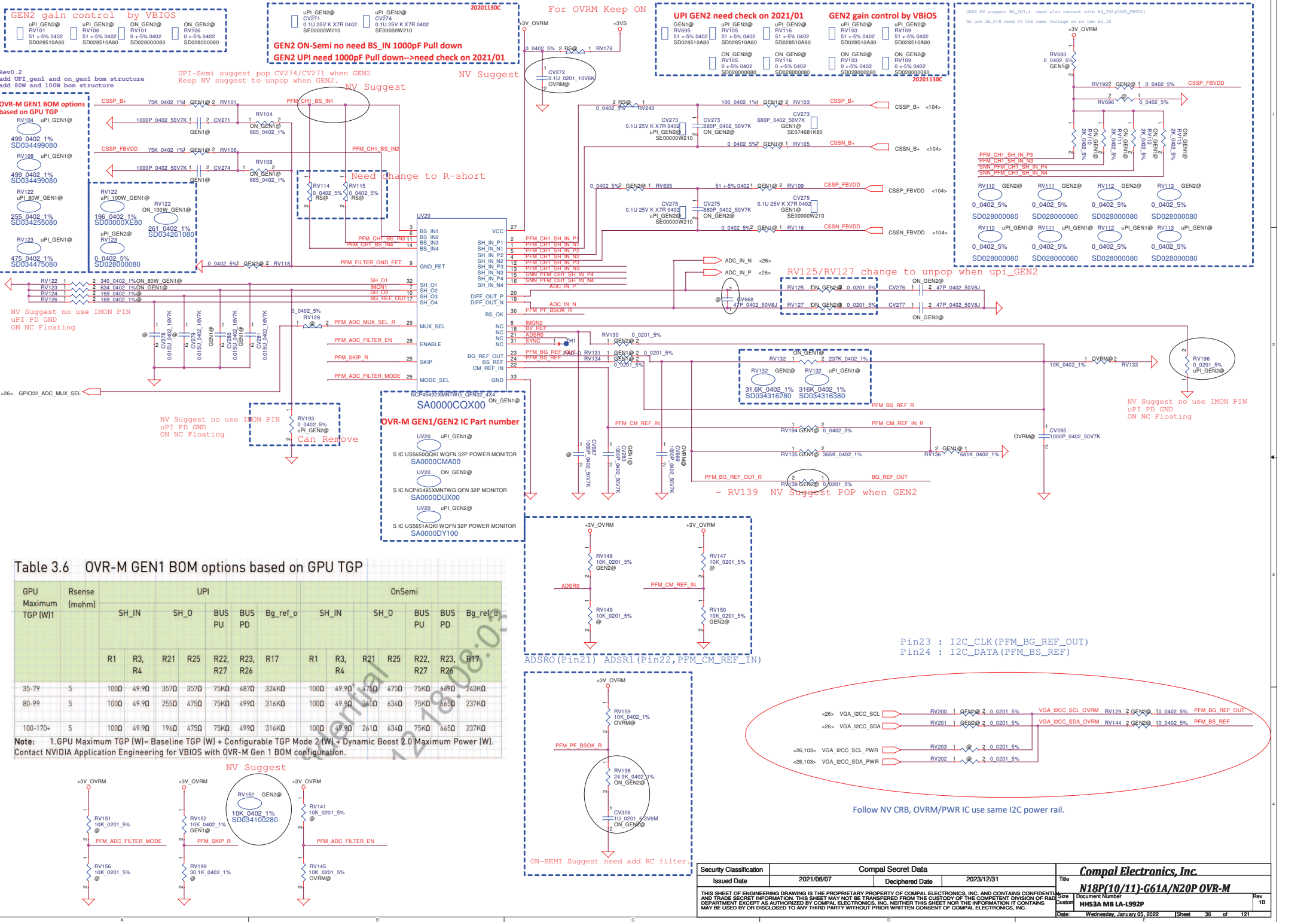
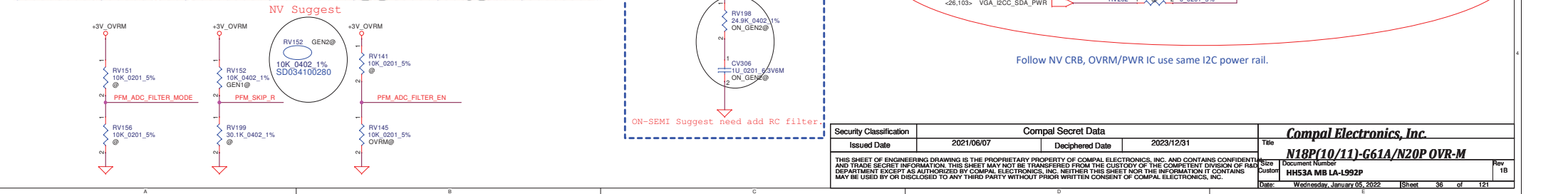
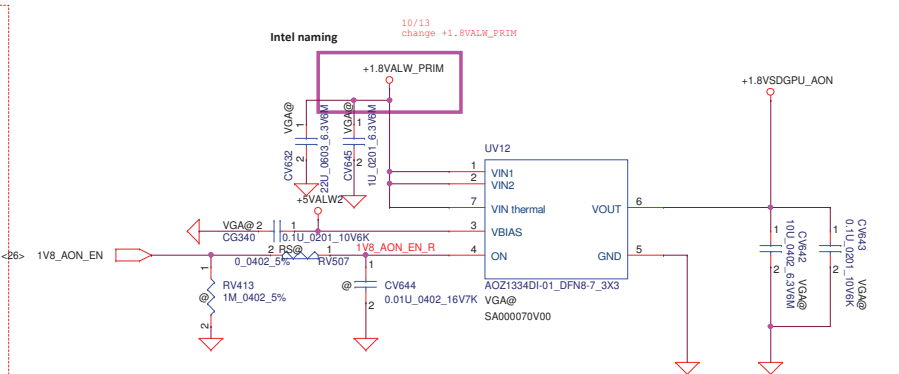
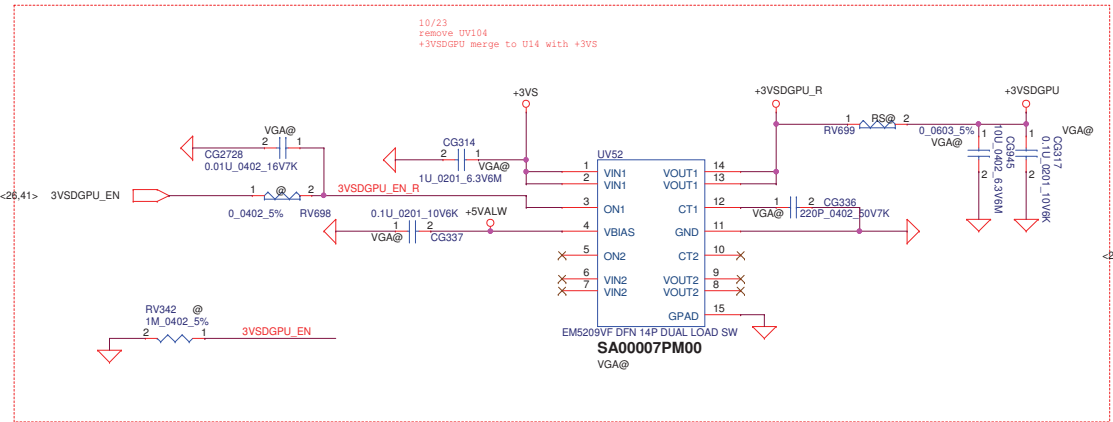


Table 3.6 OVR-M GEN1 BOM options based on GPU TGP

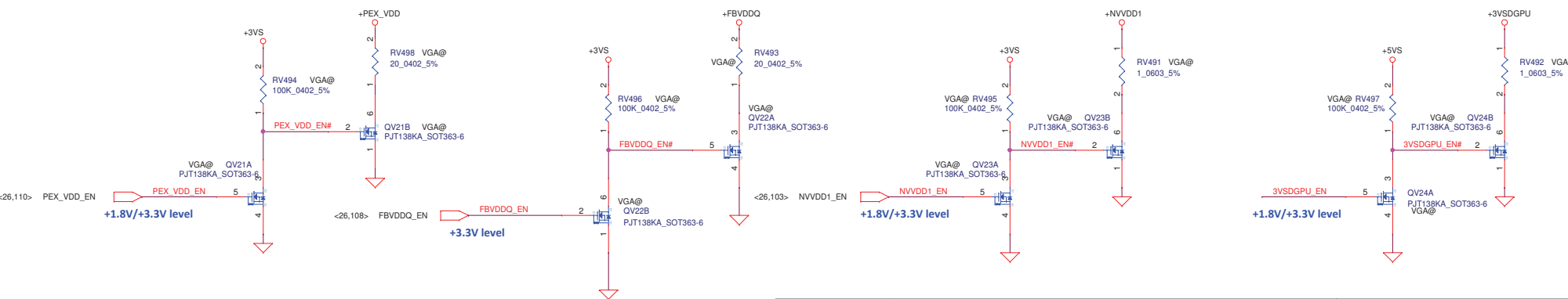
GPU Maximum TGP (W)	R _{sense} (mohm)	UPI										OnSemi						
		SH_IN		SH_O	BUS PU		BUS PD	Bg_ref_o	SH_IN	SH_O	BUS PU	BUS PD	Bg_ref_o	SH_IN	SH_O	BUS PU	BUS PD	Bg_ref_o
		R1	R3, R4	R21	R25	R22, R27	R23, R26	R17	R1	R3, R4	R21	R25	R22, R27	R23, R26	R17	R1	R3, R4	R21
35-79	5	100K	49.9K	357K	357K	75K	487K	324K	100K	49.9K	475K	475K	649K	243K				
80-99	5	100K	49.9K	255K	475K	75K	499K	316K	100K	49.9K	340K	634K	75K	665K	237K			
100-170+	5	100K	49.9K	196K	475K	75K	499K	316K	100K	49.9K	261K	634K	75K	665K	237K			

Note: 1. GPU Maximum TGP (W) = Baseline TGP (W) + Configurable TGP Mode 2 (W) + Dynamic Boost 2.0 Maximum Power (W). Contact NVIDIA Application Engineering for VBIOS with OVR-M Gen 1 BOM configuration.



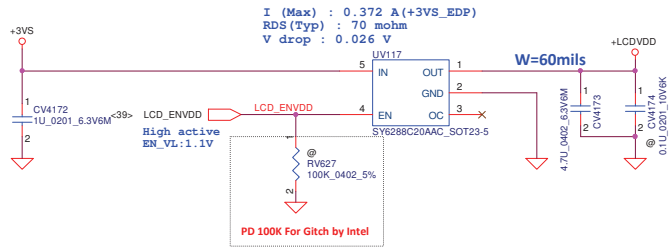


For Power down sequence

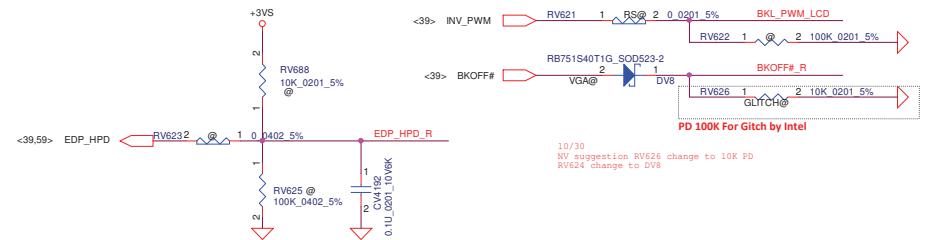


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Issued Date	2021/06/07	Deciphered Date	2023/12/31	Title	GN20E-GPU Power control
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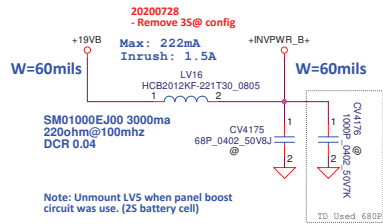
LCD POWER CIRCUIT



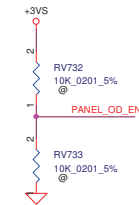
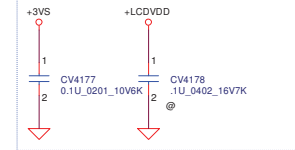
LCD enable signal



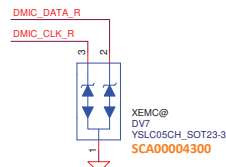
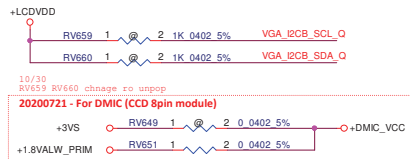
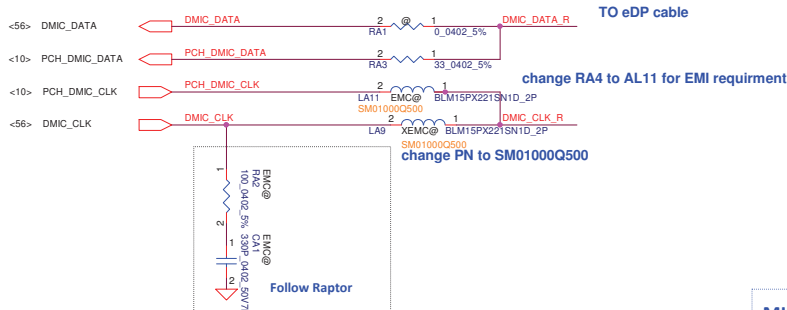
Camera



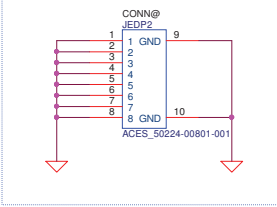
Place closed to JEDP1



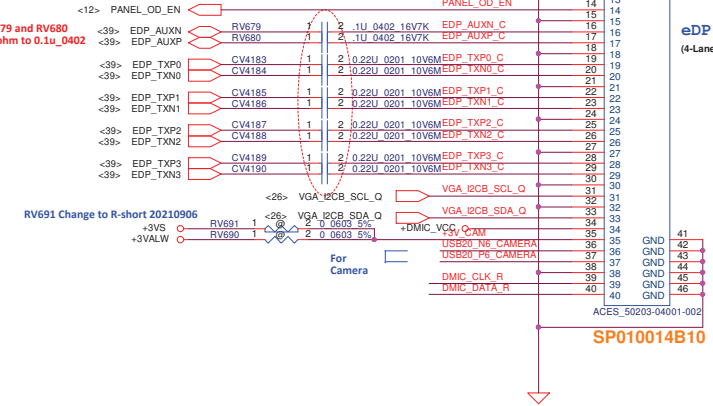
10/30 Del RV642 RV643 it already on page 39 RV567 RV568



MINILED Conn.

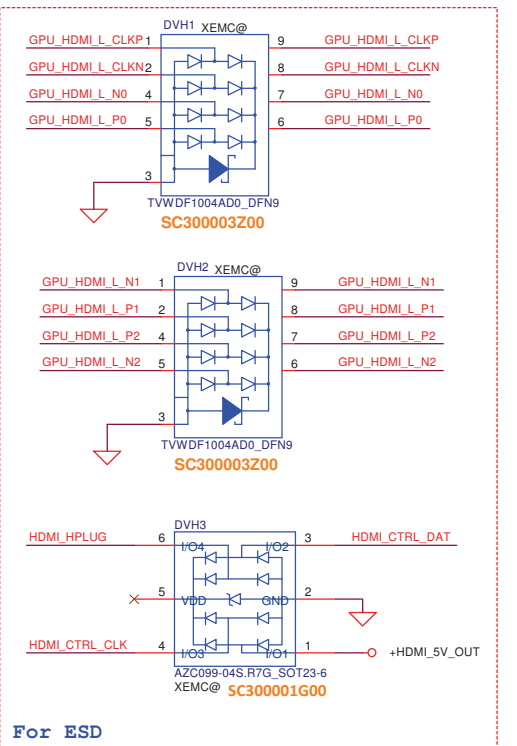
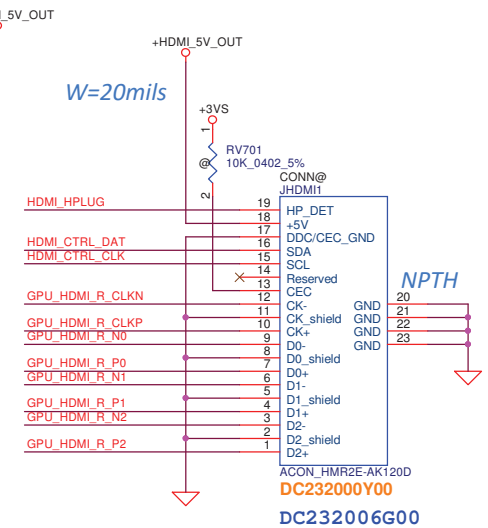


2021/4/27 RV679 and RV680 change from 0ohm to 0.1u_0402



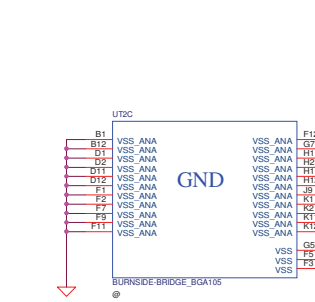
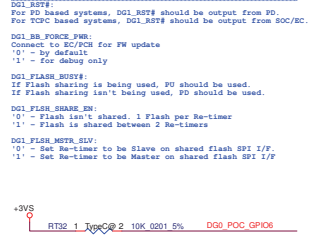
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```
Reservel for HDMI2.0
HDMI2.0 Rs=6.04 ohm(By Test)
HDMI2.1 use 0ohm(Default Use)
```



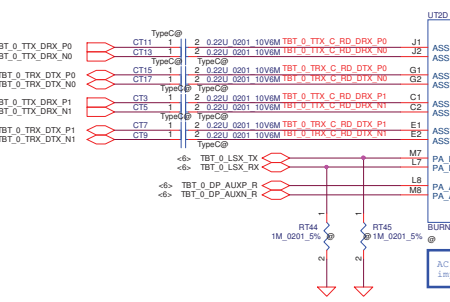
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+3VALW
 RT4 1 10K 0201 5%
 RT5 2 10K 0201 5%
 RT6 2 100 0201 1%
 RT7 2 10K 0201 5%
 SOC DG_BB FORCE PWR_R
 DG0_TEST PWR_GOOD
 DG0_POC GPIO5



The diagram shows a 25MHz crystal oscillator circuit. A crystal labeled 'Y1 TypeC@ 25MHz 10PF EX500A-CG03482' is connected between pins 1 and 3 of a package. Pin 2 is connected to ground. Pin 4 is connected to a 100nF capacitor, which is then connected to ground. A 100nF capacitor is also connected between pins 1 and 2. A note on the right states: 'Must use Metal shielded crystal for better noise immunity. Suggest adding GND shield across Crystal and 10pF caps for better RFI.' The entire circuit is enclosed in a red rectangular shield.

Diagram illustrating the removal of the JTAG connector. The circuit shows a 10k Ohm resistor connected to a 5V supply. The other end of the resistor is connected to a 2-pin header. The header pins are labeled: Pin 1 is 'Type2 @ RT56' and Pin 2 is 'Type2 @ RT57'. Below the header, there are labels for the JTAG signals: 'D00_JTAG TDI', 'D00_JTAG TMS', 'D00_JTAG TCK', and 'D00_JTAG TDO'. The header is connected to a 2-pin connector labeled 'remove connector 2/14'.

[illegible][illegible]

**Follow Burnside Bridge Rev0.84
change J5 pin to NC**

VCC3P3_SX → E6 +3VS_RETIMER

VCC3P3_SVR → M4 +3VS_RETIMER
→ M5 +0.9V0_VBT_0_5%

VCC3P3_S1R → J5 -5V

VCC3P3A → L1 +3VS_RETIMER

SVR_IND → M1 +3VS_RETIMER

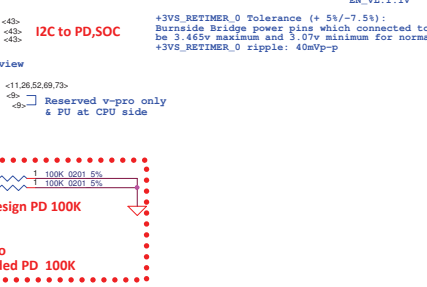
SVRL_IND → M2 +3VS_RETIMER

SVRL_VSS → M3 +3VS_RETIMER

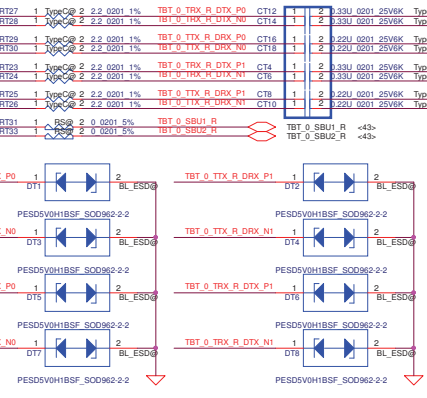
SVR_VSS → M3 +3VS_RETIMER

NC_J6 → J6 NC_J6 → RT363 0.0201_5% → GND

20200929A
- Pin "NC_J6" need NC (TBT SCH check label Rev)



NOTE:
Re-Timer with TBT , AC Caps should be use 0201/25V package.
Re-Timer without TBT , AC Caps can be use 0402/25V package.
For non-PD support 25V rating is no must.

[illegible]

Follow Burmide Bridge
Ref Schematic

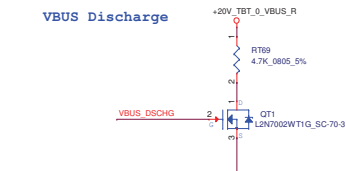
Place holder for RC filter to reduce
ripple to VCC3v3A pin



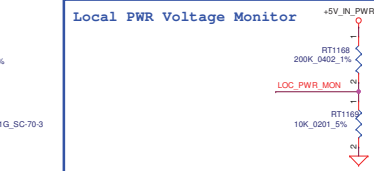
The diagram shows a close-up of a pin header labeled 'VCC3v3A'. Two pins are visible, labeled '2' and '1'. A capacitor, labeled 'C136 100nF', is connected between these two pins. The capacitor is a small, rectangular component with two leads. The text 'Follow Burmide Bridge Ref Schematic' is written above the capacitor, and 'Place holder for RC filter to reduce ripple to VCC3v3A pin' is written below it.

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				Date:	Wednesday, January 05, 2022	Sheet

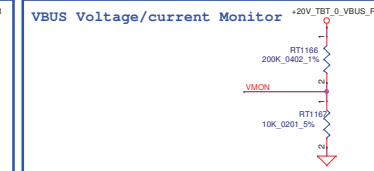
VBUS Discharge



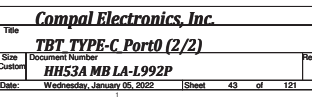
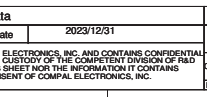
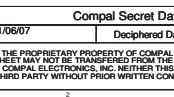
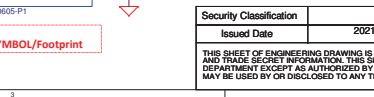
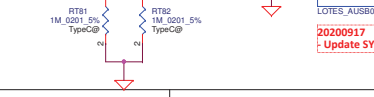
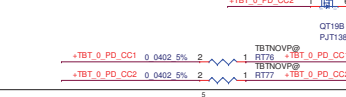
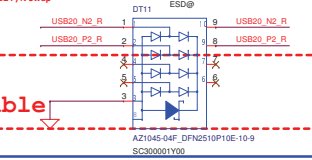
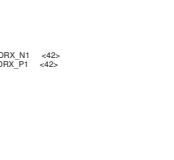
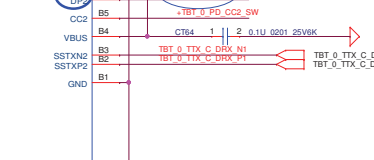
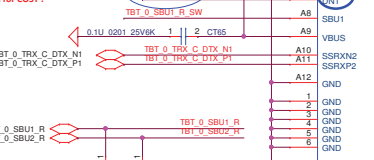
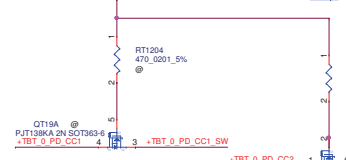
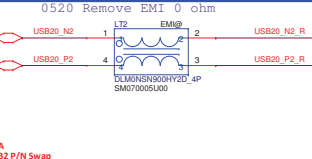
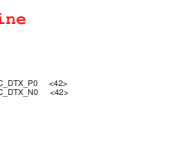
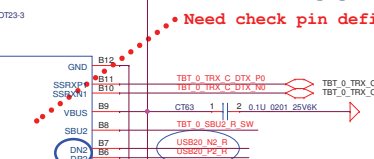
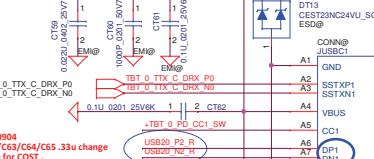
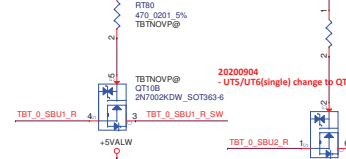
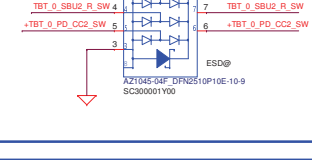
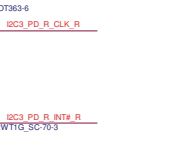
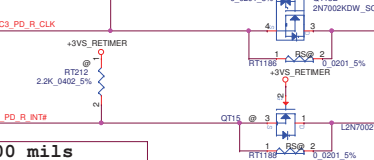
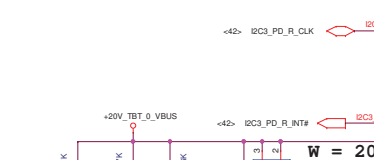
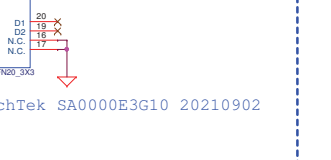
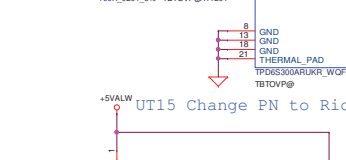
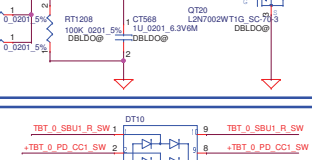
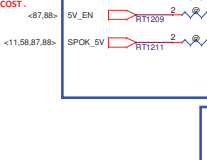
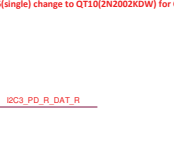
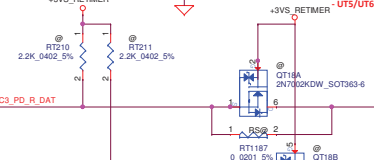
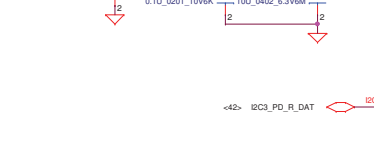
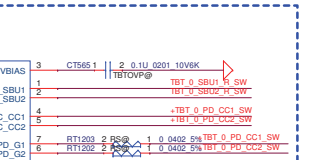
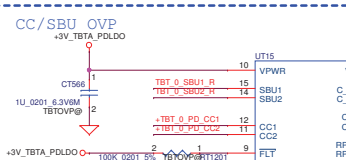
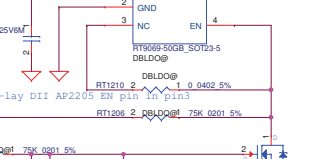
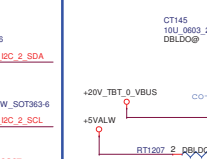
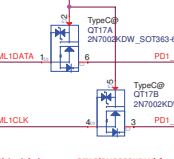
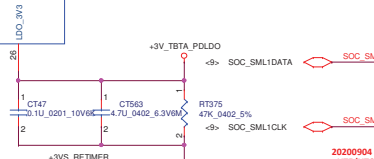
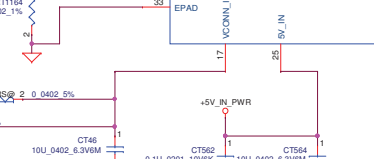
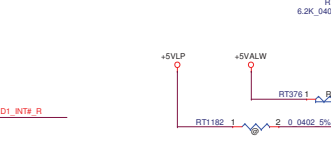
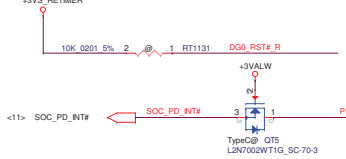
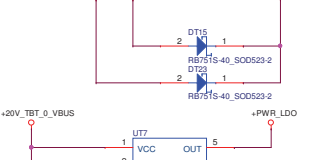
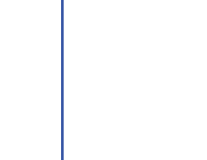
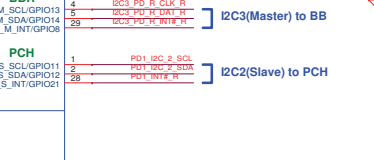
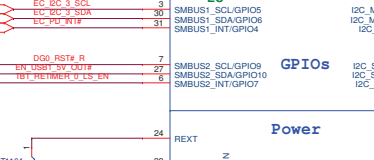
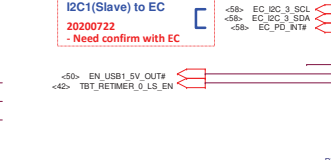
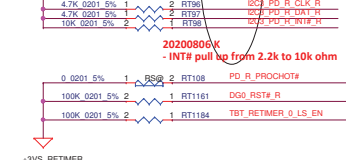
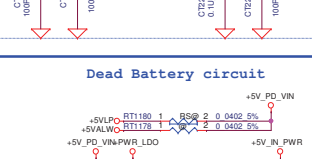
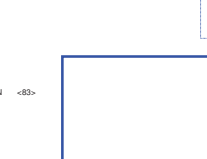
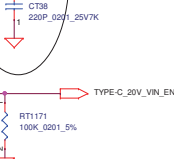
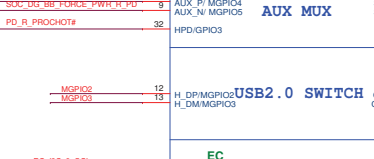
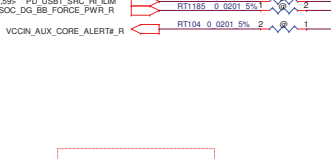
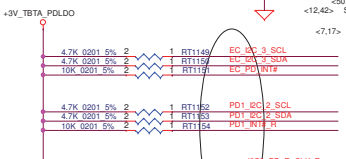
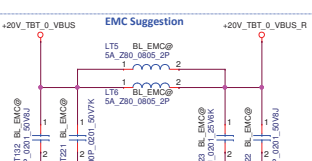
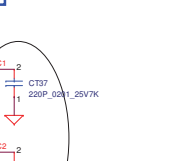
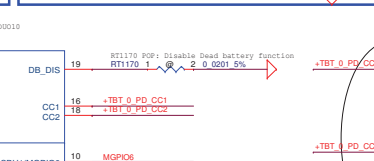
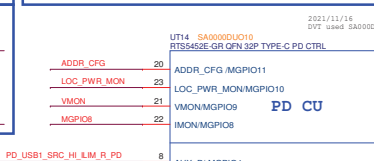
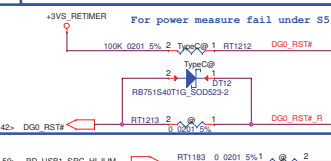
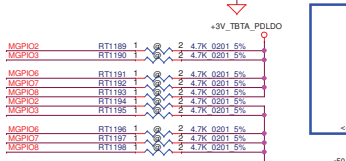
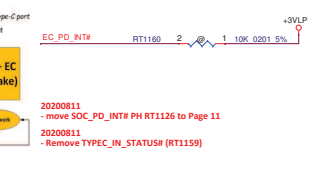
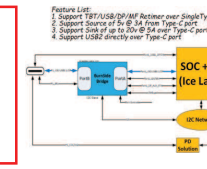
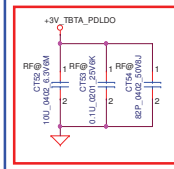
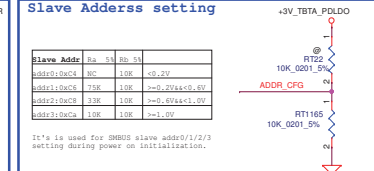
Local PWR Voltage Monitor



VBUS Voltage/current Monitor



Slave Address setting



Need check pin define

W = 200 mils

20200904 - C52/C63/C64/C65 .33u change to .1u for COST.

20200904 - U75/U76(single) change to QT10(2N2002KDW) for COST.

20200904 - U75/U76(single) change to QT10(2N2002KDW) for COST.

20200904 - U75/U76(single) change to QT10(2N2002KDW) for COST.

20200904 - U75/U76(single) change to QT10(2N2002KDW) for COST.

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20200904 - U75/U76(single) change to QT10(2N2002KDW) for COST.

20200904 - U75/U76(single) change to QT10(2N2002KDW) for COST.

20200904 - U75/U76(single) change to QT10(2N2002KDW) for COST.

Reserve Page

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				Date:	Wednesday, January 05, 2022
				Sheet	44 of 121
				Rev	1B
				Document Number	HH53A MB LA-L992P

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				Date:	Wednesday, January 05, 2022
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				Rev	1B
				HH53A MB LA-L992P	

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				Date:	Wednesday, January 05, 2022
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				Date:	Wednesday, January 05, 2022
				Sheet	47 of 121
				Rev	1B
				Document Number	HH53A MB LA-L992P

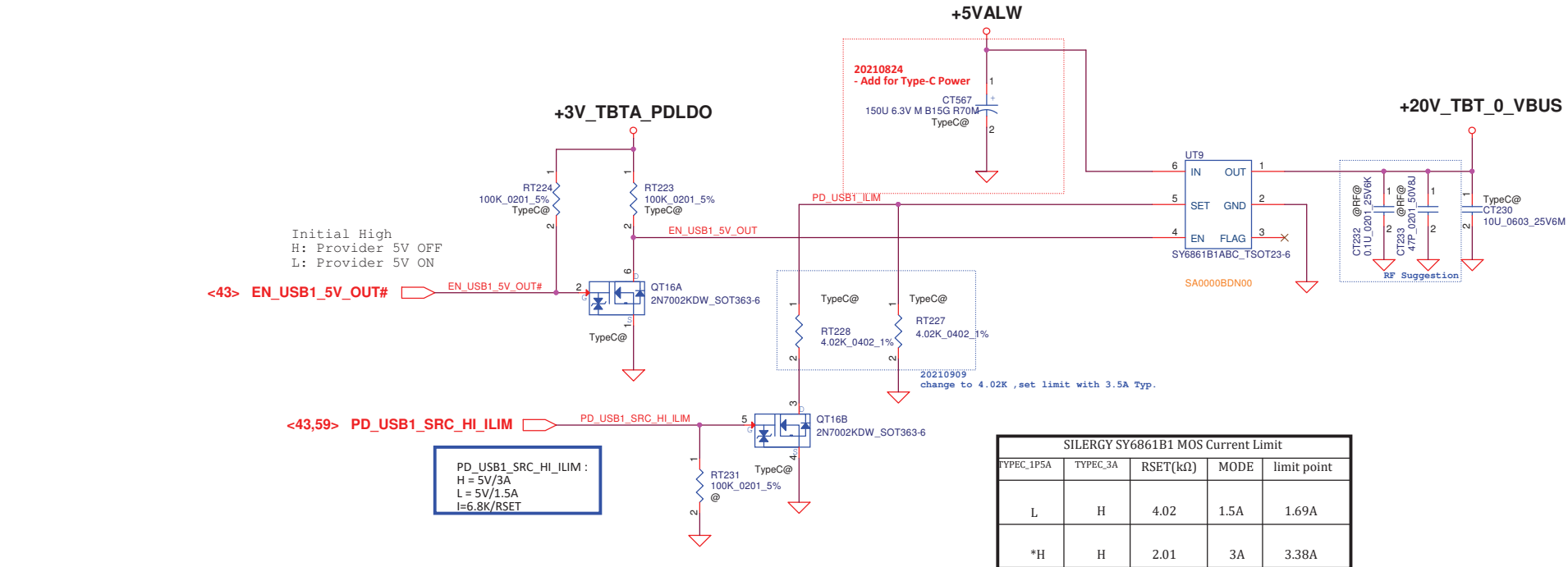
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				Date:	Wednesday, January 05, 2022
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				Document Number	HH53A MB LA-L992P

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				Date:	Wednesday, January 05, 2022
				Sheet	49 of 121
				Rev	1B
				HH53A MB LA-L992P	

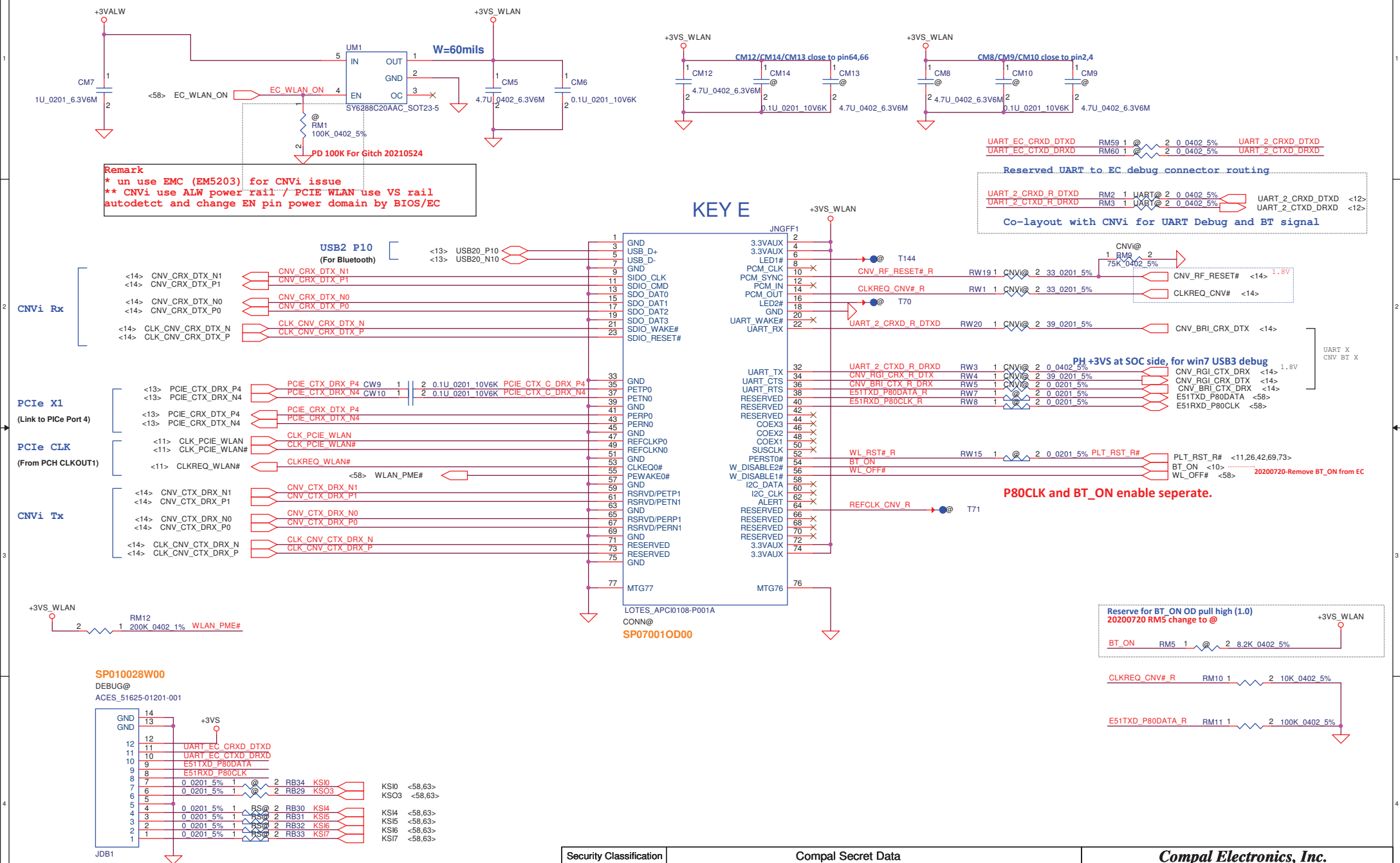
MB_USB3.1 TypeC Conn. (Power Path)
- For Realtek 5452E



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NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



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					Size	Document Number	Rev
						HH53A MB LA-L992P	1B
Date:					Wednesday, January 05, 2022	Sheet	52 of 121

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				Date:	Wednesday, January 05, 2022
				Sheet	53 of 121
				Rev	1B
				HH53A MB LA-L992P	

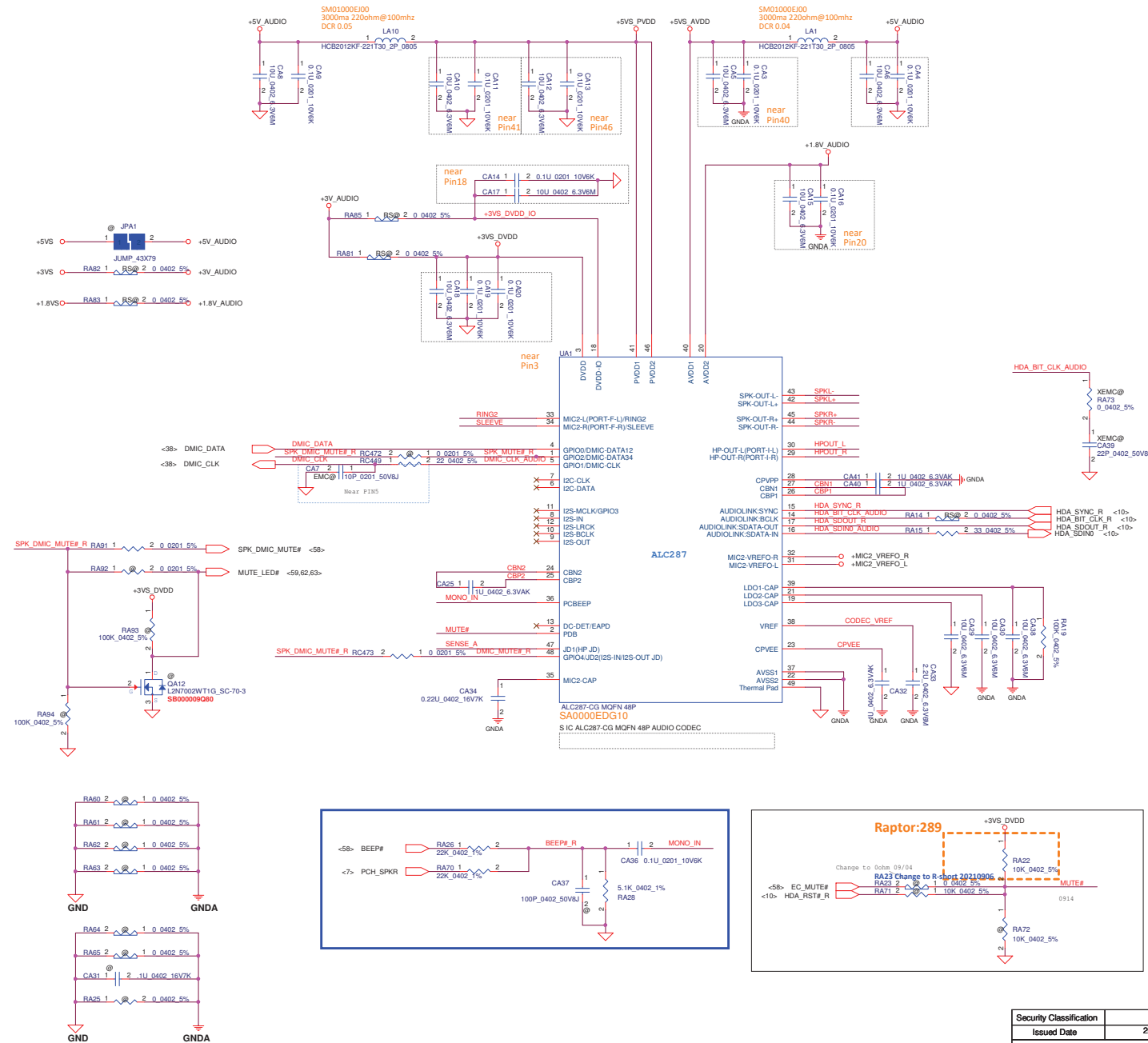
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				HH53A MB LA-L992P	
				Date:	Wednesday, January 05, 2022
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				Rev	1B

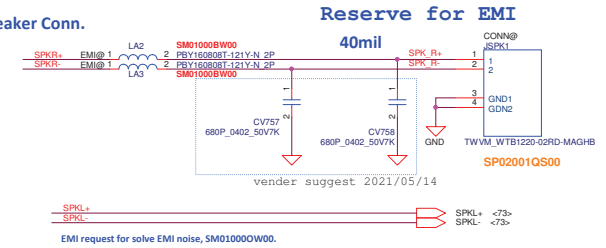
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				Date:	Wednesday, January 05, 2022
				Sheet	55 of 121
				Rev	1B
				HH53A MB LA-L992P	

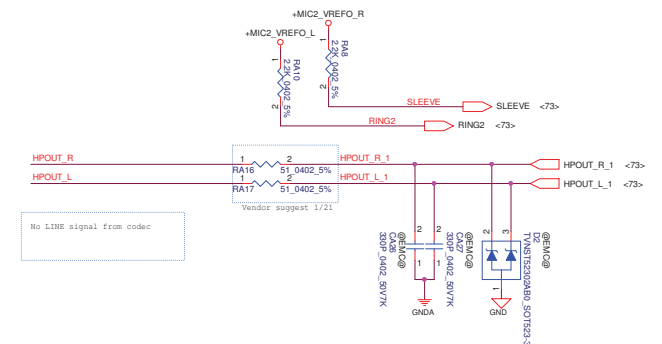
HD Audio Codec



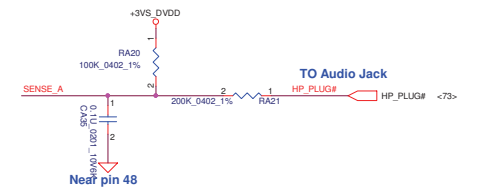
Int. Speaker Conn.



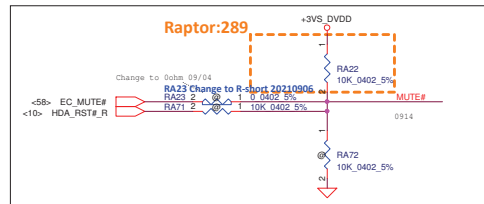
Headphone Out



JACK Detect



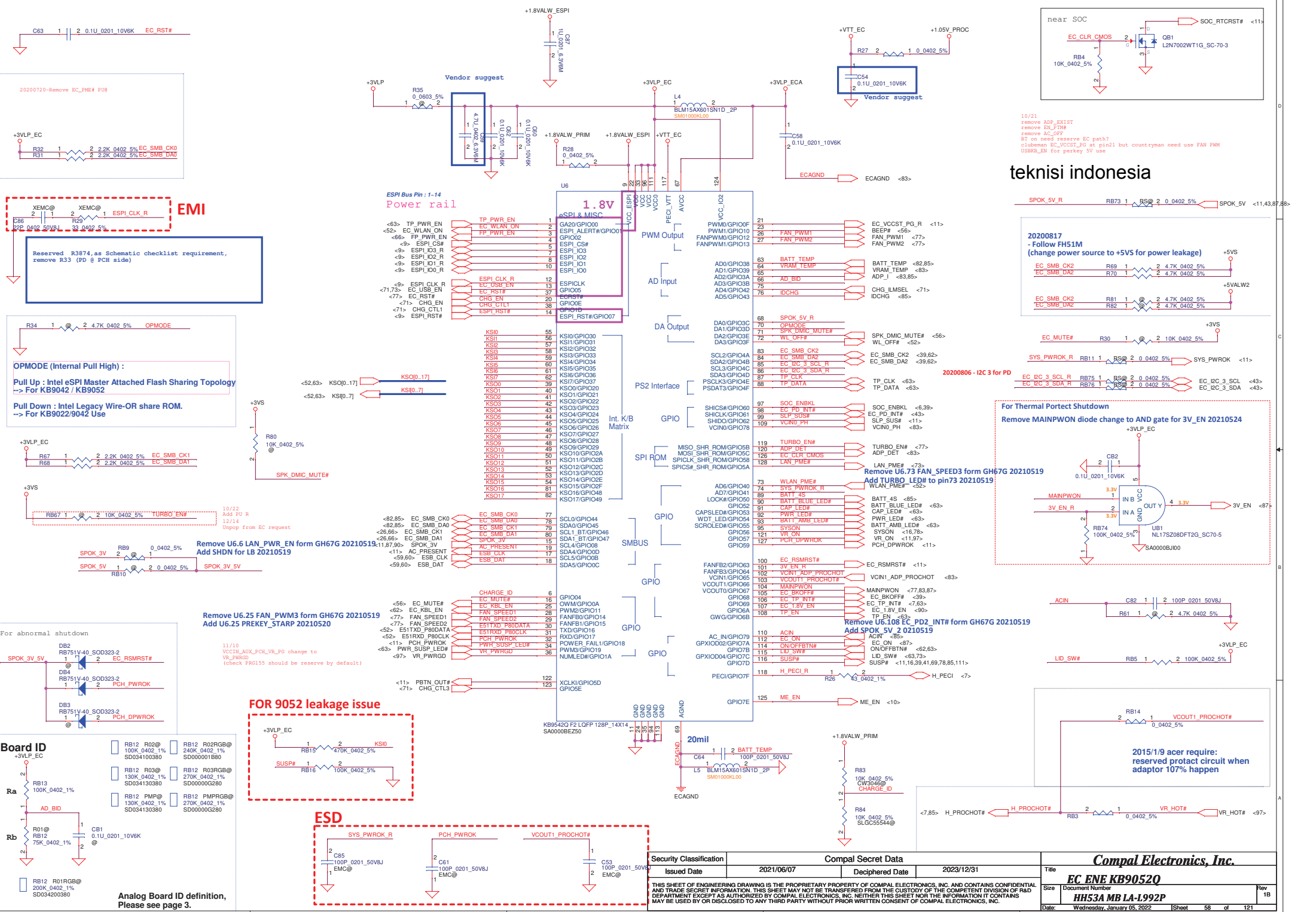
Raptor:289



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Issued Date	2021/06/07	Deciphered Date	2023/12/31	Title	Audio-Reserve
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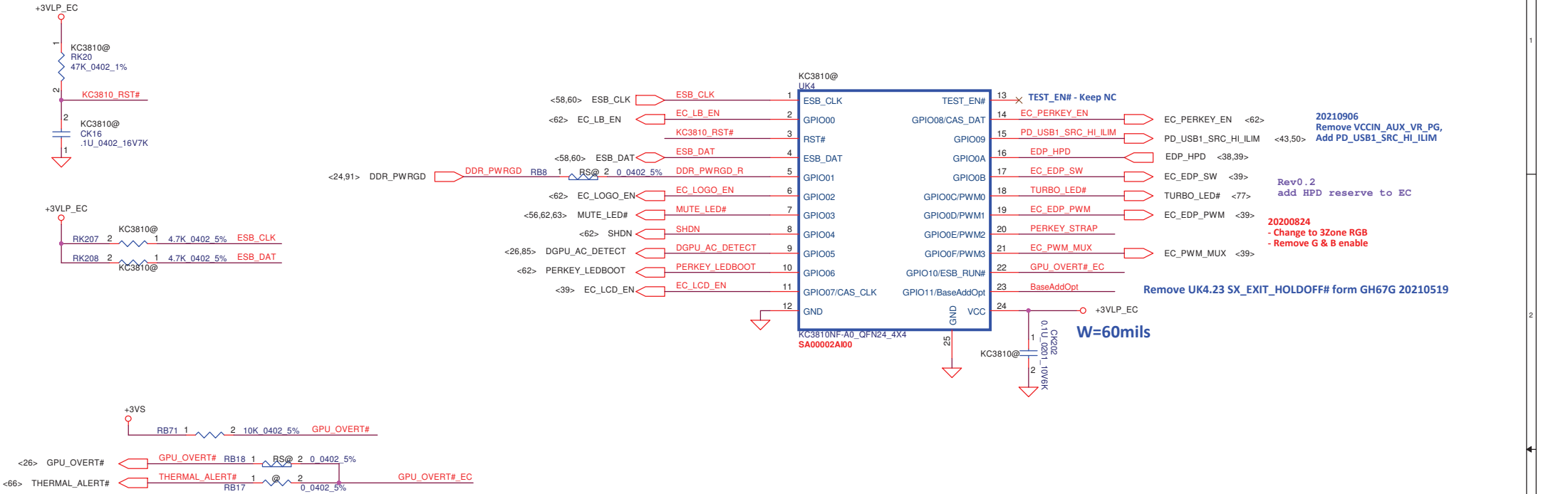


teknisi indonesia

20200720-Remove EC_PWE# PWR	
Reserved R3874, as Schematic checklist requirement, remove R33 (PD @ PCH side)	
OPMODE (Internal Pull High) : Pull Up : Intel eSPI Master Attached Flash Sharing Topology --> For KB9042 / KB9052 Pull Down : Intel Legacy Wire-OR share ROM. --> For KB9022/9042 Use	
Remove U6.25 LAN_PWR_EN form GH67G 20210519 Add SHDN for LB 20210519	
Remove U6.25 FAN_PWM3 form GH67G 20210519 Add U6.25 PREKEY_STARP 20210520	
For abnormal shutdown	
FOR 9052 leakage issue	
ESD	
Board ID	
Analog Board ID definition, Please see page 3.	
Security Classification	
Compal Secret Data	
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Title	
EC ENE KB9052Q	
Size	
HH53A MB LA-1992P	
Date	
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Sheet	
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OMEN New ESB CLK&DAT for Extend I/O

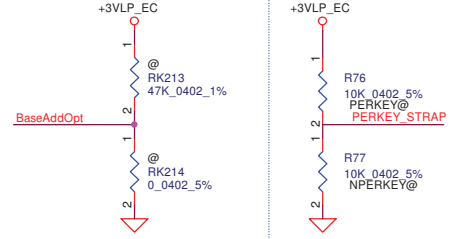
*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.



Need EC confirm

[GPIO11/BaseAddOpt]
If support second 3810,
please let one 3810 GPIO11 connect GND and
the other keep NC or initial High

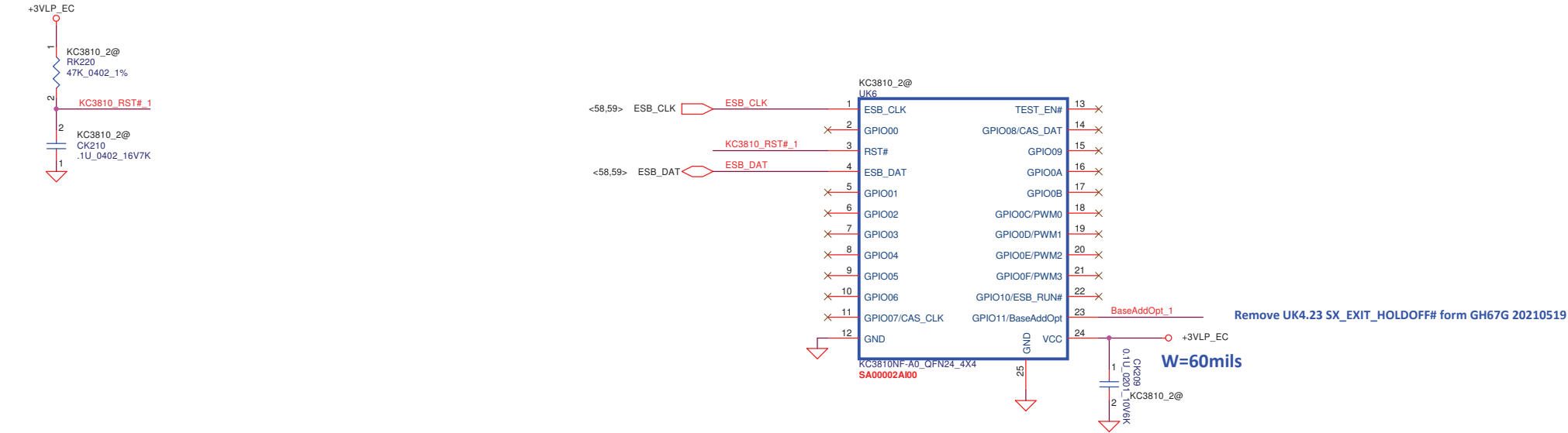
- High/NC: USR_EGPIOBaseSetting - 0x00
- Low: USR_EGPIOBaseSetting - 0x08



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				Date	Wednesday, January 05, 2022
				Sheet	59 of 121
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OMEN New ESB CLK&DAT for Extend I/O

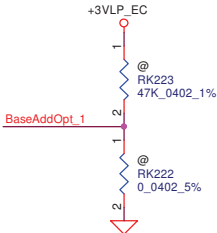
*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.



Need EC confirm

[GPIO11/BaseAddOpt]
If support second 3810,
please let one 3810 GPIO11 connect GND and
the other keep NC or initial High

- High/NC: USR_EGPIOBaseSetting - 0x00
- Low: USR_EGPIOBaseSetting - 0x08

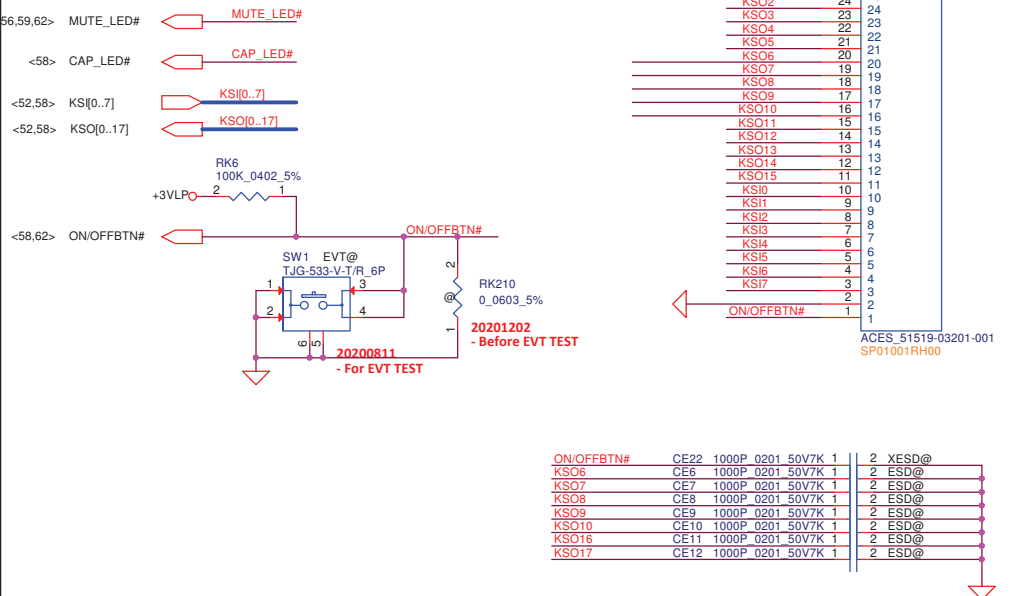


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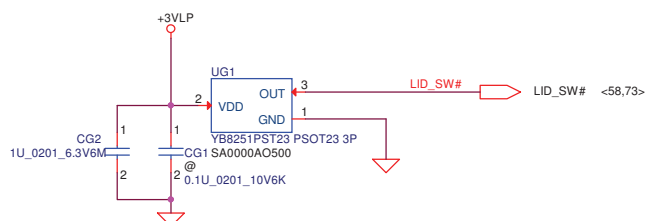
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2021/06/07	Deciphered Date	2023/12/31	Title	Reserve for SMB/I2C Block Diagrams
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ON/OFF BTN

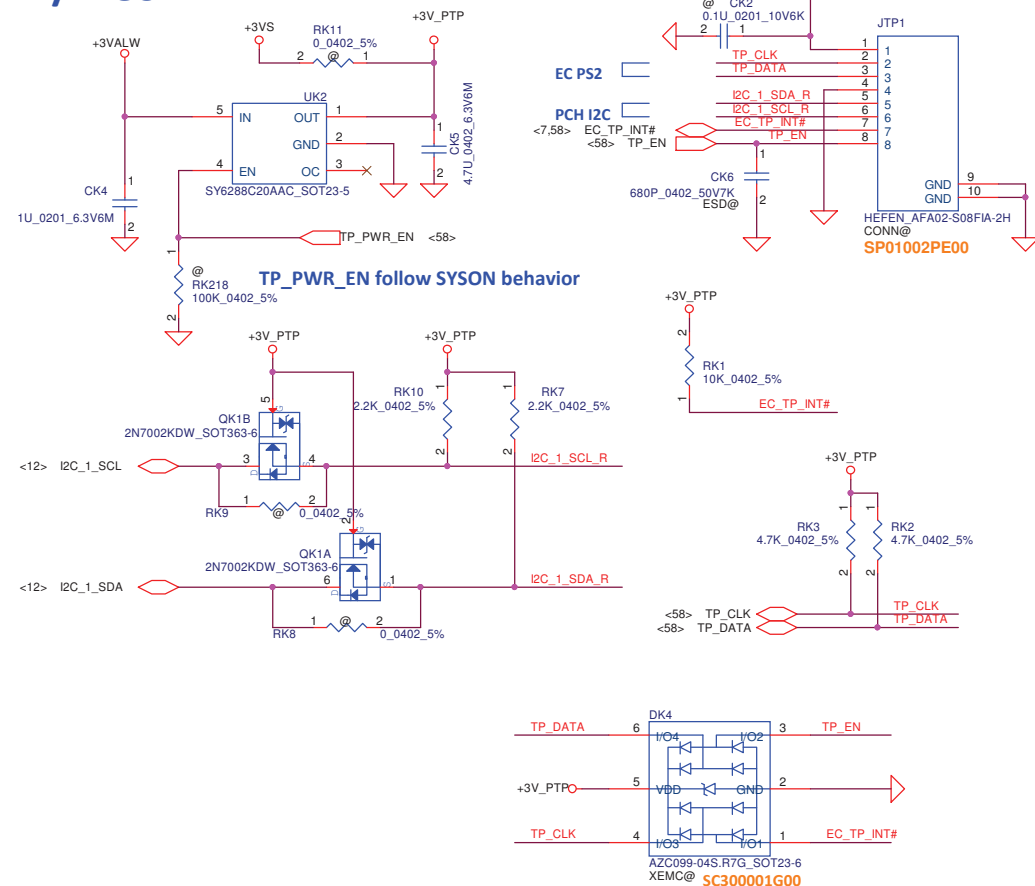


20200823
-KB BackLight (1 Zone RGB) 6pin Change to page 62

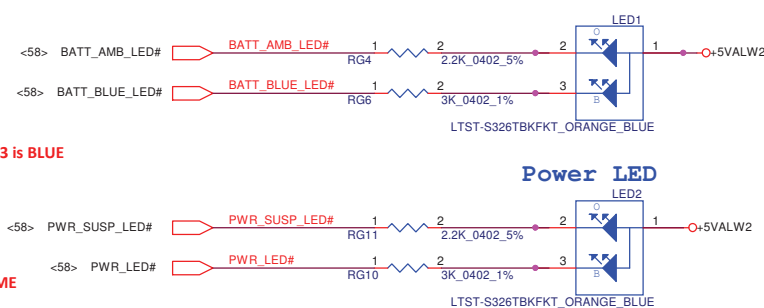
Hall sensor



TP/B Conn.



Battery LED



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Issued Date	2021/06/07	Deciphered Date	2023/12/31	Title		
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				Size	Document Number	Rev
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				Date:	Wednesday, January 05, 2022
				Sheet	64 of 121
				Rev	1B
				HH53A MB LA-L992P	

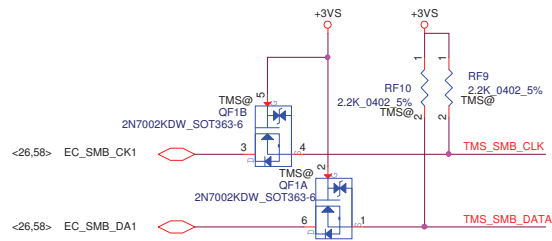
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				HH53A MB LA-L992P	
				Date:	Wednesday, January 05, 2022
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				Rev	1B

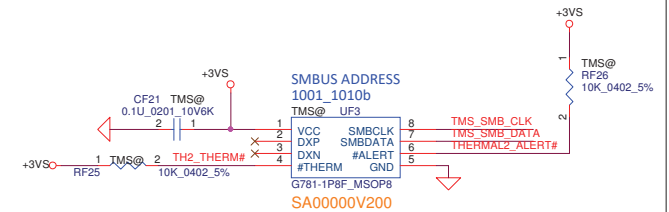
20200717
- Remove G-Sensor

THERMAL SENSOR

20200810
- Check address

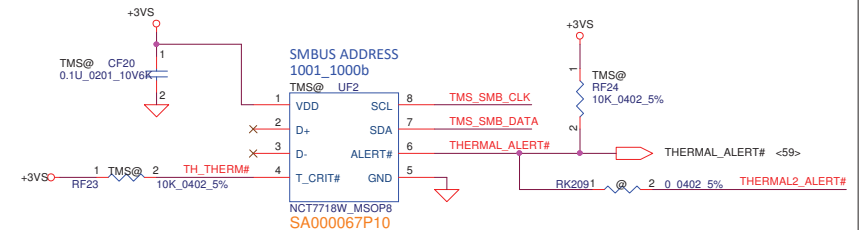


Close to Thermal SKIN



20200928
- Remove 3rd thermal sensor

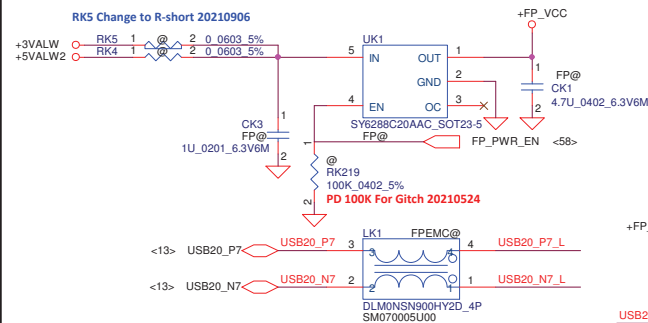
Close to SO-DIMM



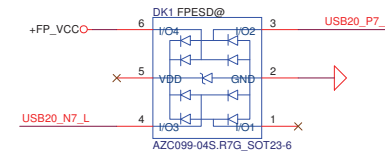
PN Change to SA000067P10 form SA000067P00
20210715

TPM 2.0

Finger print



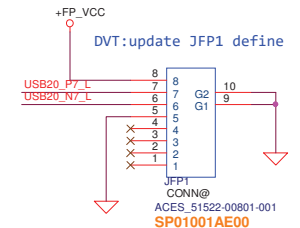
teknisi indonesia



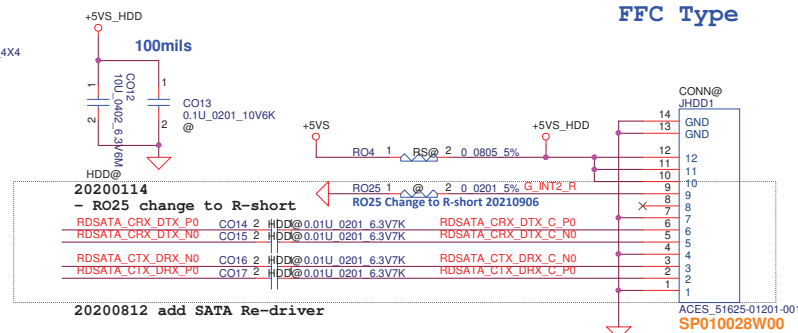
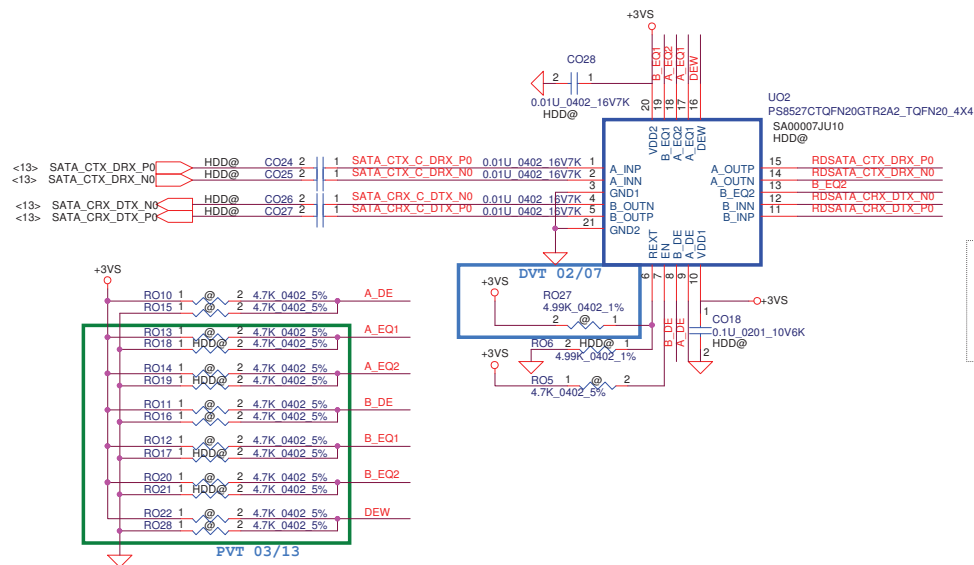
20210528 remove TPM

PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



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				Deciphered Date				2023/12/31			
								TPM/FP/Sensor			
								Document Number			
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				Date:	Wednesday, January 05, 2022
				Sheet	67 of 121
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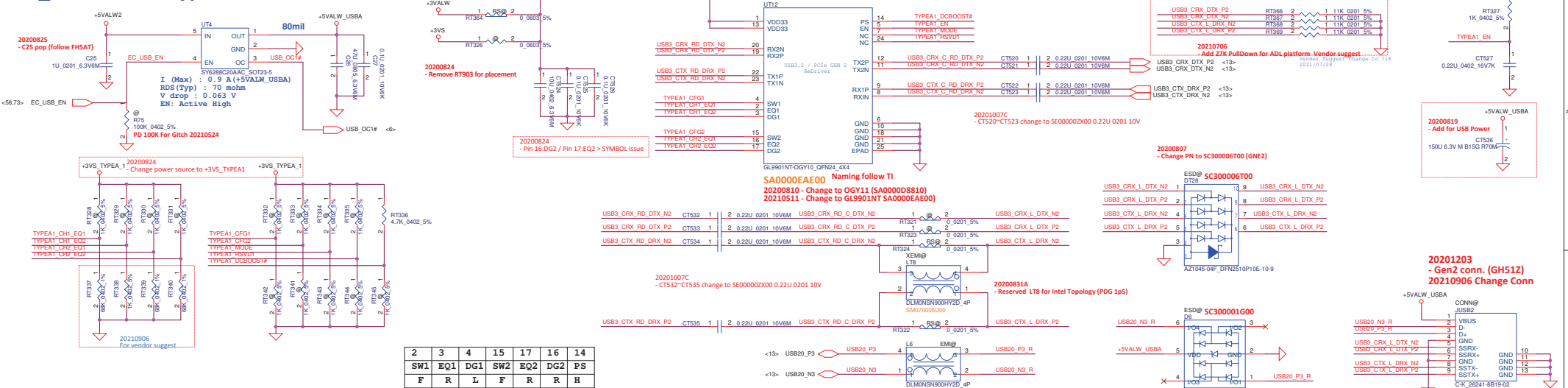
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Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2021/06/07	Deciphered Date	2023/12/31	Title	N18E-GDDR6 D
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				Date	Wednesday, January 05, 2022
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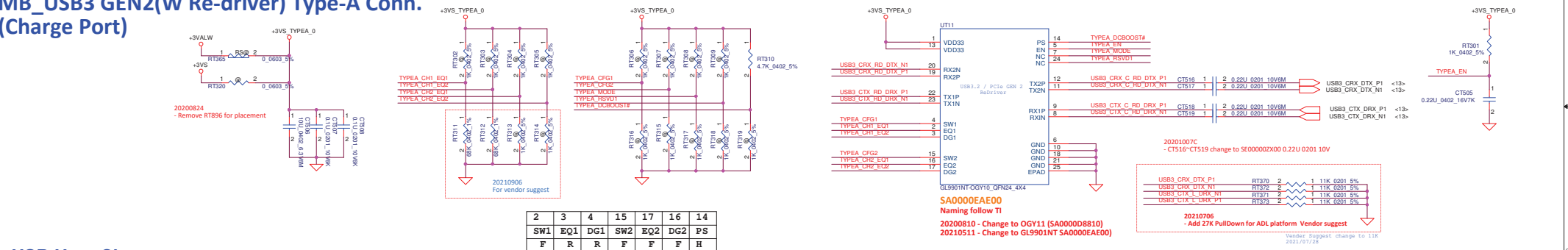
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2021/06/07	Deciphered Date	2023/12/31	Title	SATA/PCIE-SSD
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				HH53A MB LA-L992P	1B
				Date: Wednesday, January 05, 2022	Sheet 70 of 121

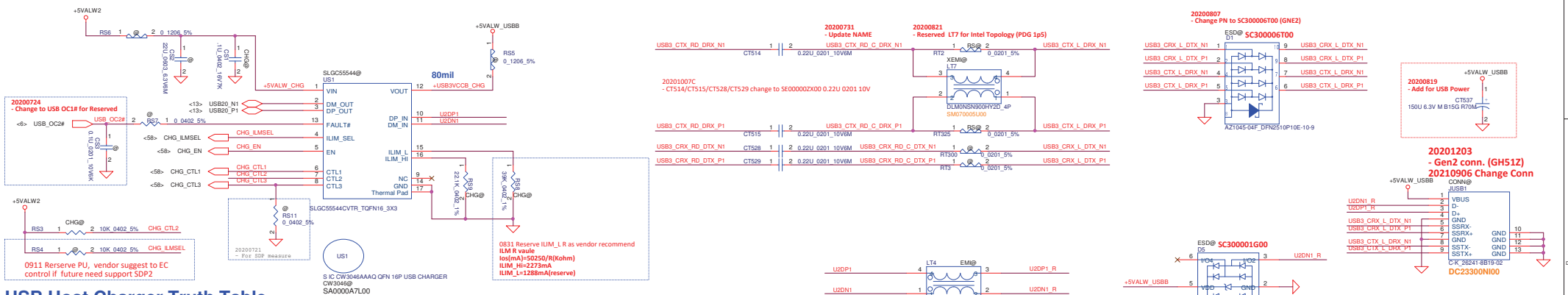
MB_USB3 GEN2 Type-A Conn.



MB_USB3 GEN2(W Re-driver) Type-A Conn. (Charge Port)



USB Host Charger



USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-0FF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

Security Classification	Compal Secret Data		Title		New 18
Issued Date	2021/08/07	Deciphered Date	2023/12/31	<i>USB2/USB3 TYPEA1&2</i> Document Number <i>HS53A MB LA-1992P</i>	
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				Date:	Wednesday, January 05, 2022
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				Rev	1B
				HH53A MB LA-L992P	

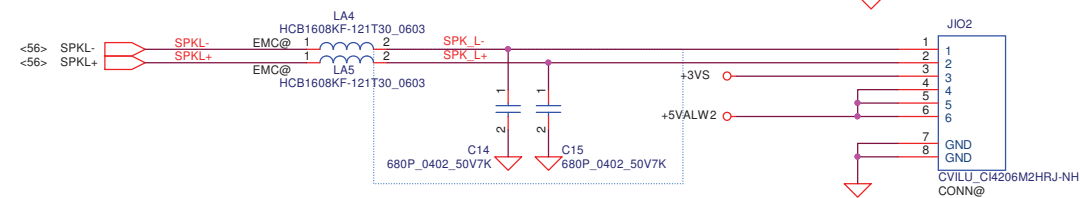
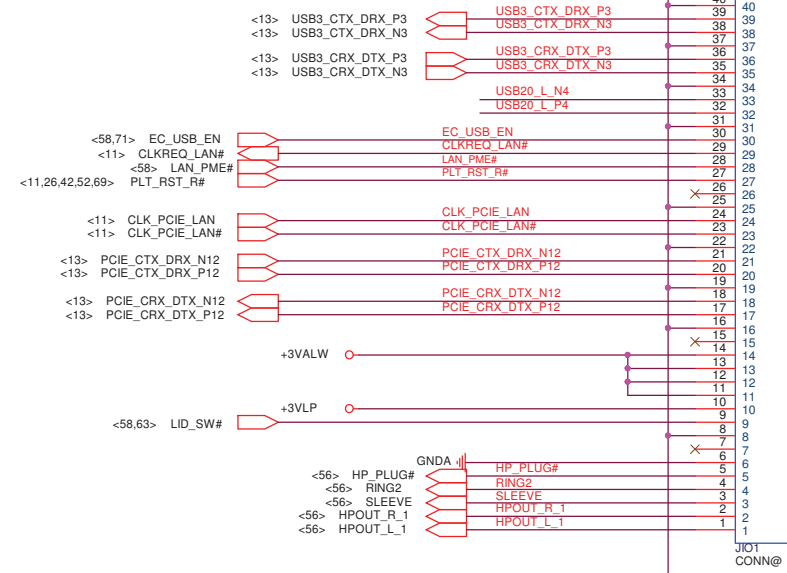
IO/B CONN



0702
- IO_B change pin define

Check IO FFC double pin location

SDAN_606044-040041



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				Date:	Wednesday, January 05, 2022
				Sheet	74 of 121
				Rev	1B
				Document Number	HH53A MB LA-L992P

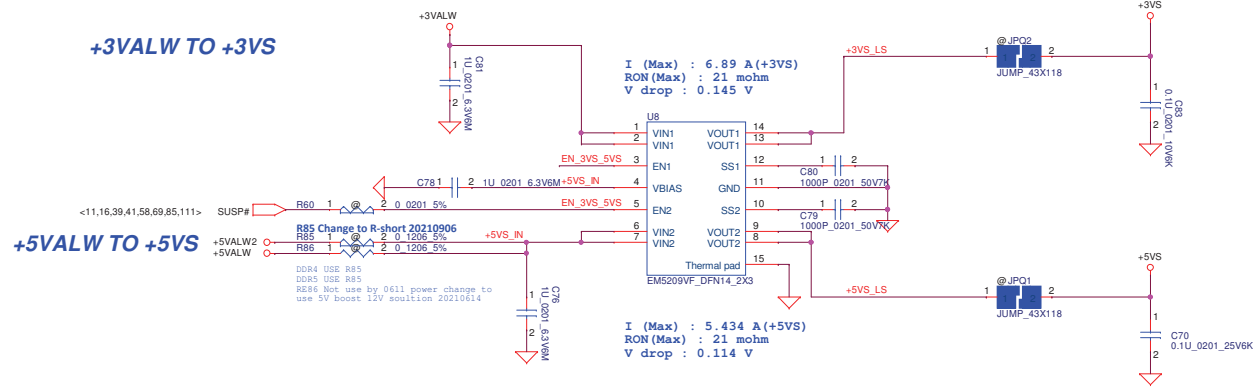
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date:	Wednesday, January 05, 2022
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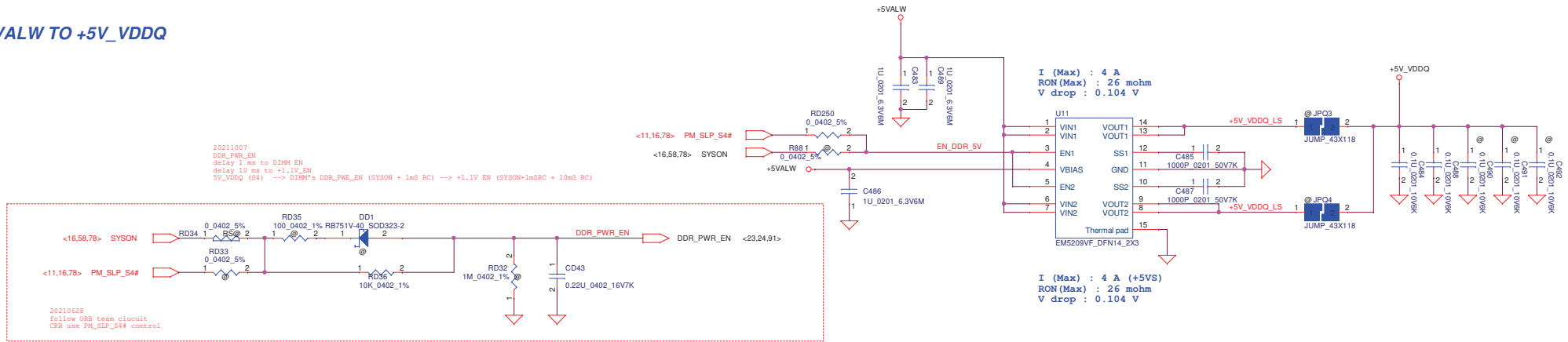
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					Size	Document Number		
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+5VALW TO +5V_VDDQ



20210604
 - Move +1.8VALW to +1.8VS to page 69

20200717
 - Remove VGA Power sequence

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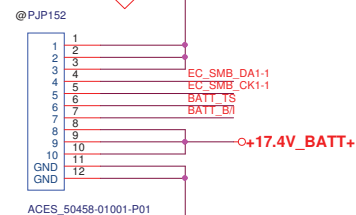
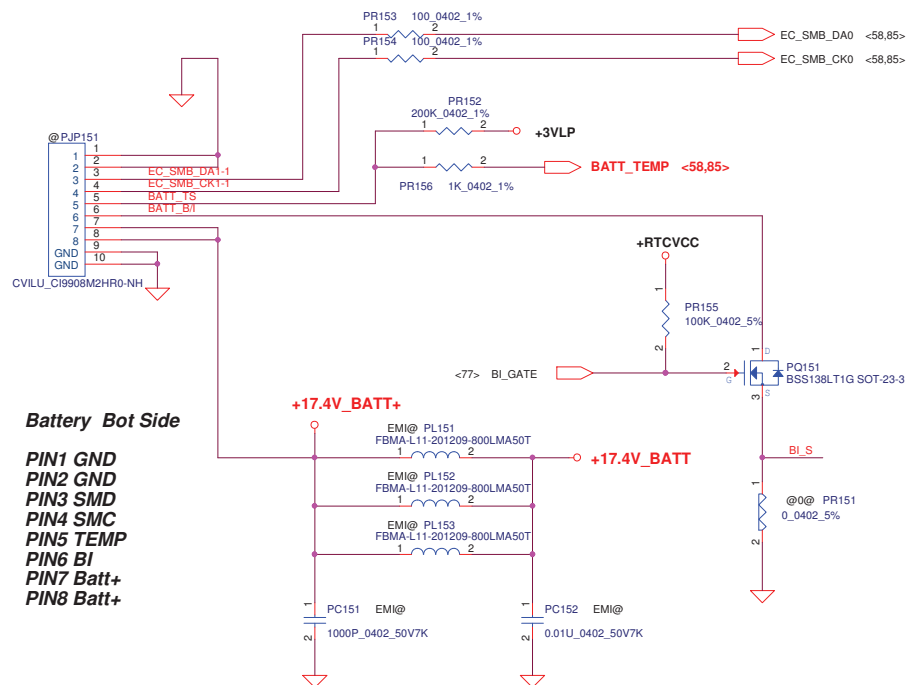
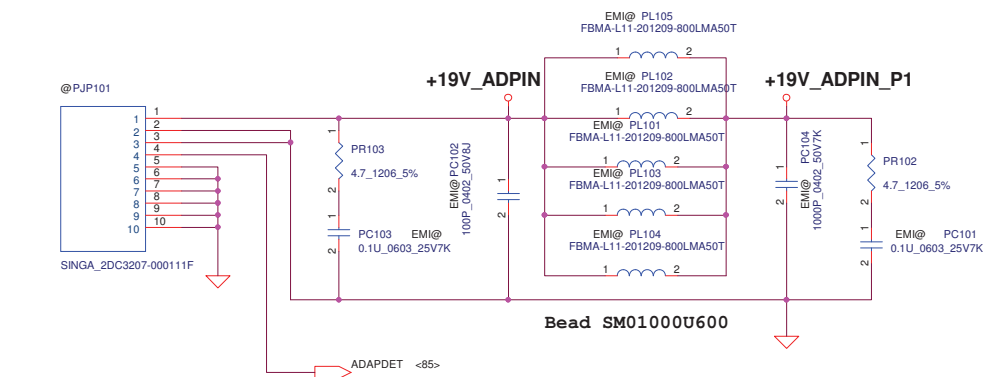
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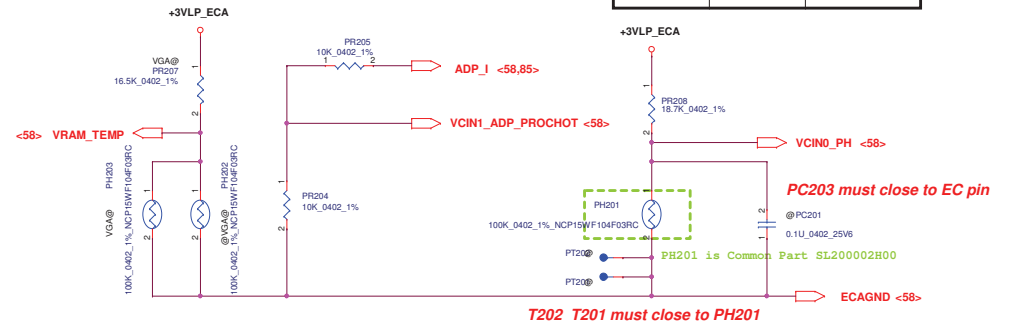
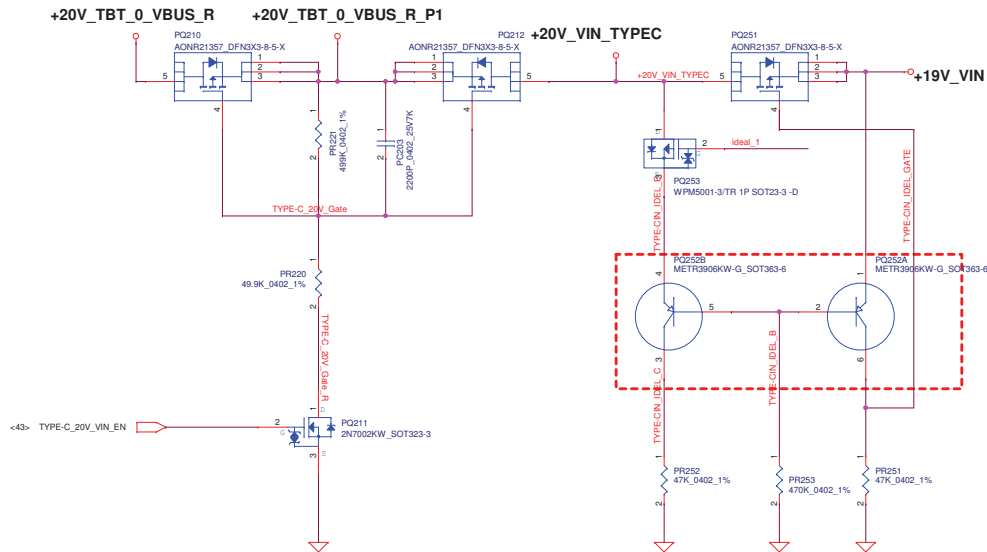
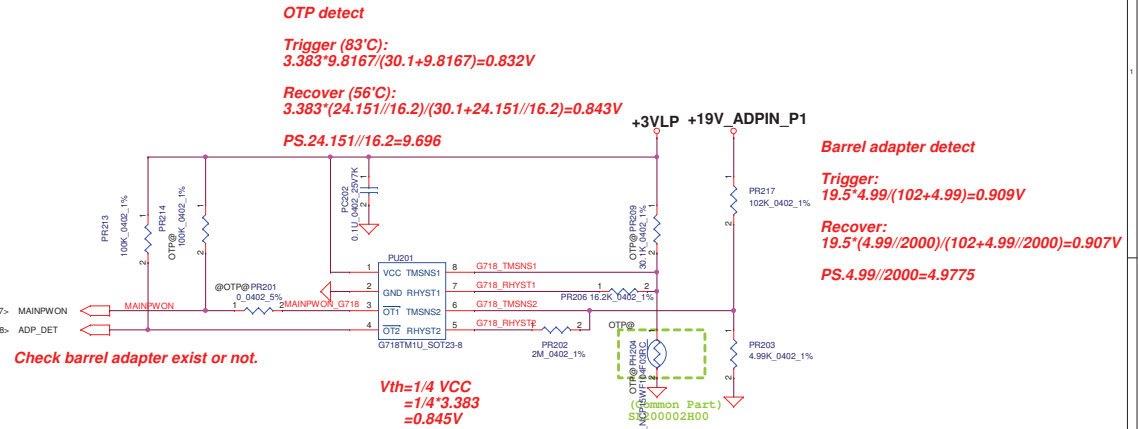
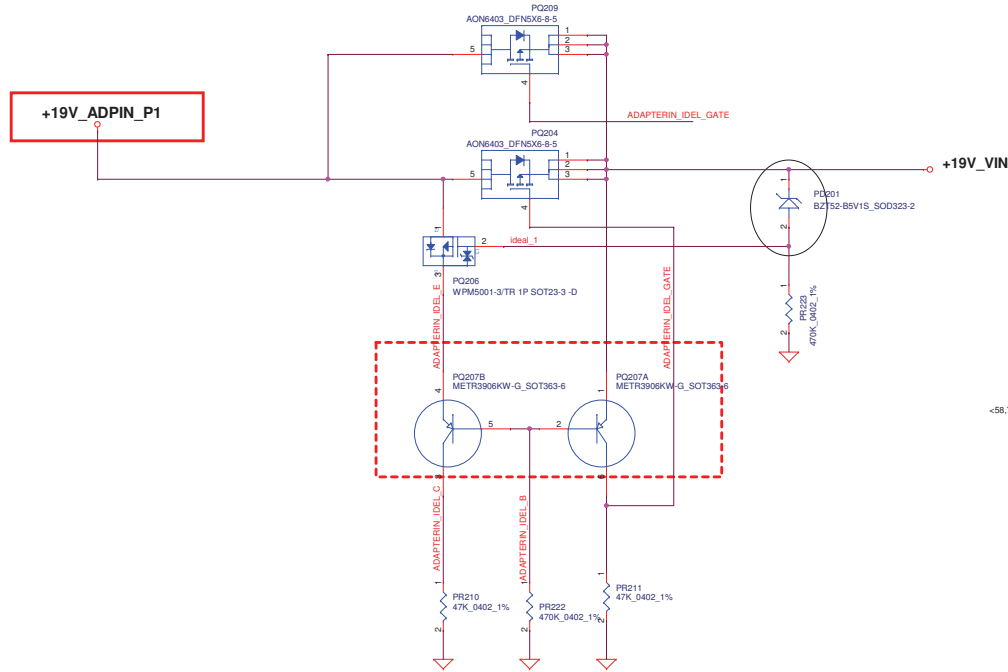
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Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+

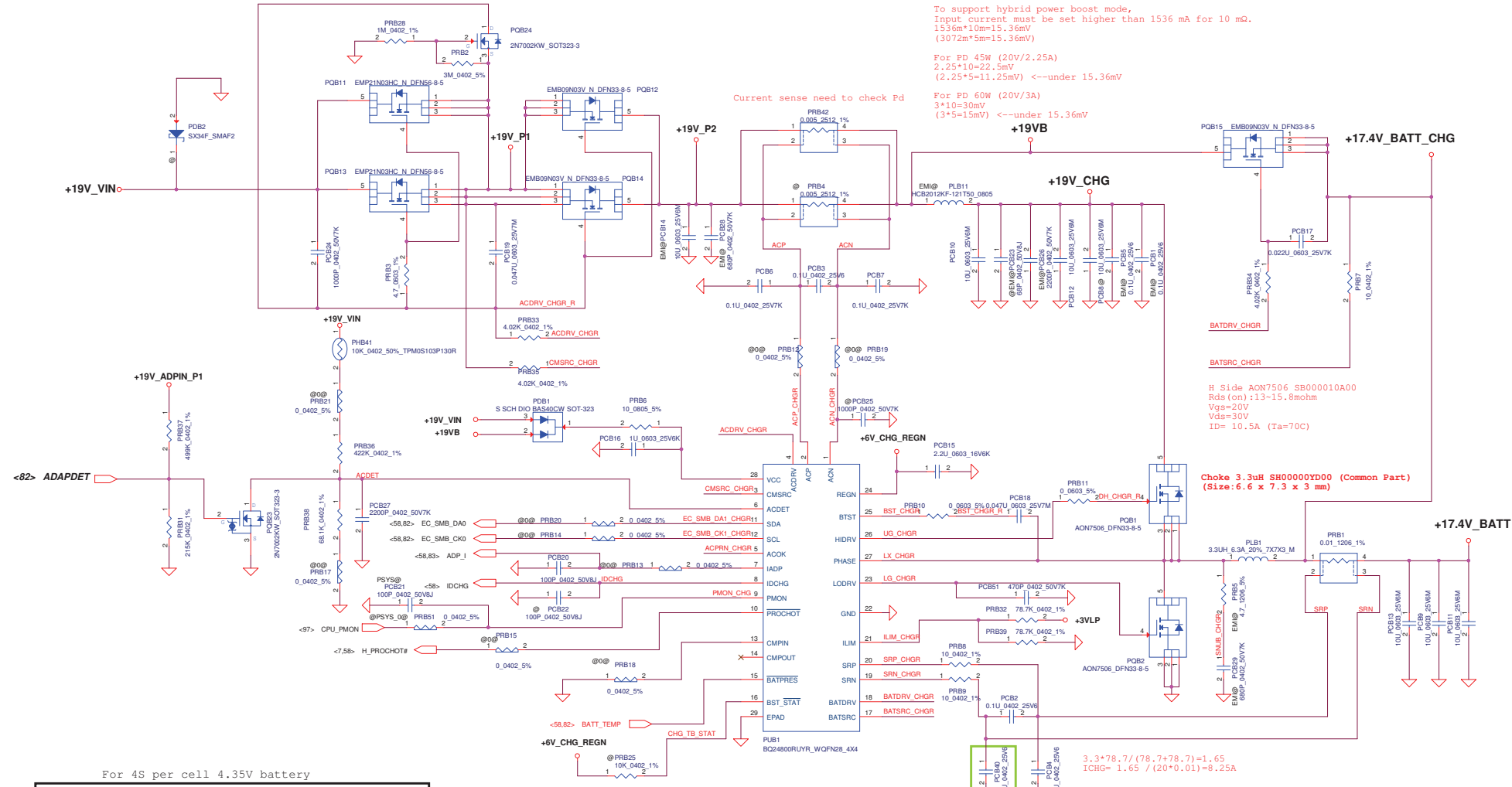
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Issued Date	2016/11/03	Deciphered Date	2017/06/14	Title	DCIN
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To support hybrid power boost mode,
 Input current must be set higher than 1536 mA for 10 mΩ.
 $1536 \text{ mA} \times 10 \text{ m}\Omega = 15.36 \text{ mV}$
 $(3072 \text{ m} \times 5 \text{ m}\Omega = 15.36 \text{ mV})$

For PD 45W (20V/2.25A)
 $2.25 \times 10 = 22.5 \text{ mV}$
 $(2.25 \times 5 = 11.25 \text{ mV})$ <---under 15.36mV

For PD 60W (20V/3A)
 $3 \times 10 = 30 \text{ mV}$
 $(3 \times 5 = 15 \text{ mV})$ <---under 15.36mV

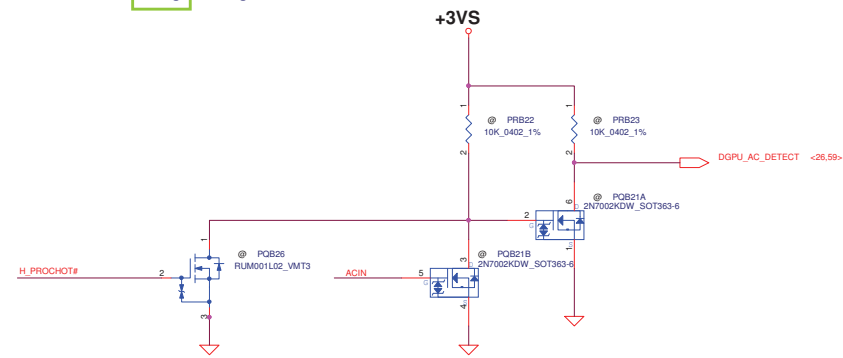
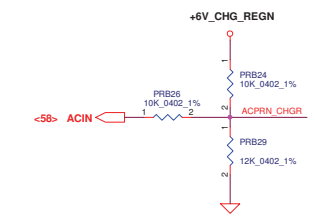
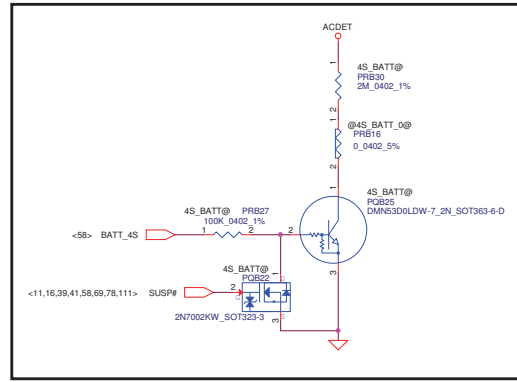
H Side AON7506 SB000010A00
 $R_{ds(on)}: 13-15.8 \text{ m}\Omega$
 $V_{gs} = 20 \text{ V}$
 $V_{ds} = 30 \text{ V}$
 $I_D = 10.5 \text{ A}$ ($T_a = 70^\circ \text{C}$)

Choke 3.3uH SH00000YD00 (Common Part)
 (Size: 6.6 x 7.3 x 3 mm)

$$3.3 \times 78.7 / (78.7 + 78.7) = 1.65$$

$$\text{ICHG} = 1.65 / (20 \times 0.01) = 8.25 \text{ A}$$

For 4S per cell 4.35V battery

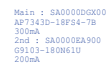
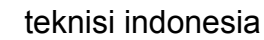


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Security Classification	Compal Secret Data		Title	
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			HH53A MB LA-L992P	1B
			Date: Wednesday, January 05, 2022	Sheet 89 of 121

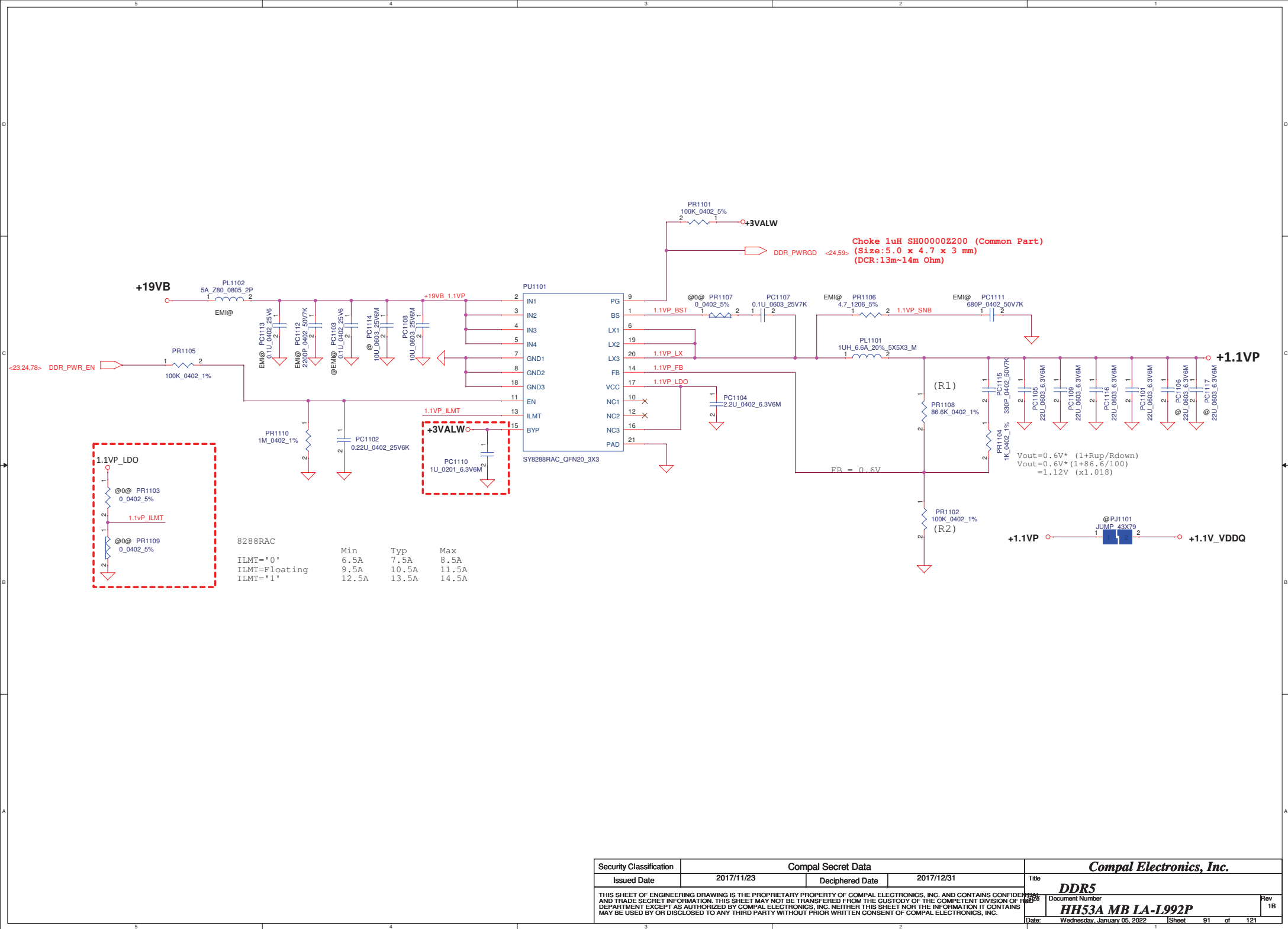


Compal Electronics, Inc.

1.8V

Document Number	HH53A MB LA-L992P
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10



Security Classification		Compal Secret Data		<div> <div>Compal Electronics, Inc.</div> <div> <div>Title</div> <div>DDR5</div> </div> <div> <div>Document Number</div> <div>HH53A MB LA-L992P</div> </div> <div> <div>Date:</div> <div>Wednesday, January 05, 2022</div> </div> <div> <div>Sheet</div> <div>91 of 121</div> </div> </div>	
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3		2			

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				Date:	Wednesday, January 05, 2022	Sheet 93 of 121

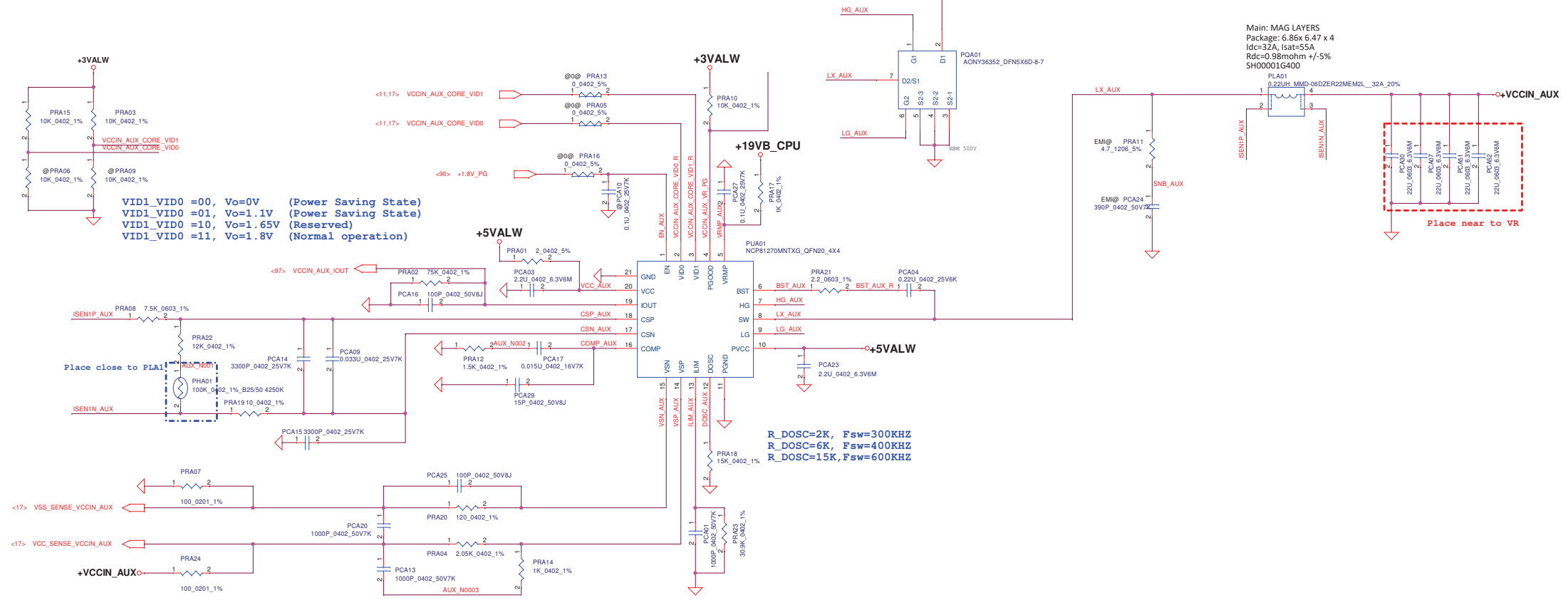
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				C	HH53A MB LA-L992P	1B
Date: Wednesday, January 05, 2022				Sheet	94	of 121

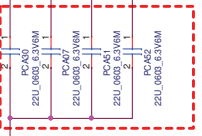
Main Func = +VCCIN_AUX

+VCCIN_AUX
Vout 1.8V
IPL2(TDC) = 17A (->BIOS set up x8)
Peak Current = 34.2A (ICCmax) (->BIOS set up x4)
DC Load line: 2.0mohm (->BIOS set up x100)
AC Load line: 3.4mohm (->BIOS set up x100)
OCP: 44.6 A
OVP: VID+0.36V (max 2V)
FSW= 600KHz

2021/09/08
Delete VCCIN_AUX_VR_PG by HW request
To used for RTS5452E current limit.



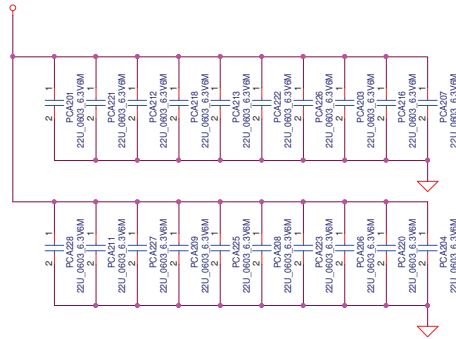
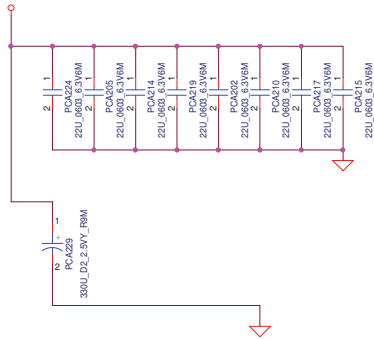
Main: MAG LAYERS
Package: 6.86x6.47 x 4
Idc=32A, Isat=55A
Rdc=0.98mohm +/-5%
SH00001G400



R_DOSC=2K, Fsw=300KHz
R_DOSC=6K, Fsw=400KHz
R_DOSC=15K, Fsw=600KHz

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Issued Date		2021/01/07		Deciphered Date		2021/01/07		Title		PWR_AUX/AUX_PCH/DECOUPLING	
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Size		Document Number		H4514 MB LA-1972P						Rev 1B	
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330uF_2.5V*1
22uF_0603*28



Security Classification		Compal Secret Data		Compal Electronics, Inc. PWR VCCIN AUX DECOUPLING	
Issued Date	2020/02/27	Deciphered Date	2021/12/31	Title	
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					HHS14 MB LA-1372P
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Main Func = CPU (IA/GT)

+VCC_CORE
IPL2 = 93A (->BIOS set up x8)
Peak Curren = 160A (ICCMAX) (->BIOS set up x4)
DC Load line: 2.3mohm (->BIOS set up x100)
AC Load line: 2.3mohm (->BIOS set up x100)
Current limit = 200A (OCP)
OVP = VID+0.36V
FSW= 540K Hz
Vboot: 0V

+VCC_GT
IPL2 = 30A (->BIOS set up x8)
Peak Curren = 55A (ICCMAX) (->BIOS set up x4)
DC Load line: 3.2mohm (->BIOS set up x100)
AC Load line: 3.2mohm (->BIOS set up x100)
Current limit = 71A (OCP)
OVP = VID+0.36V
FSW= 540K Hz
Vboot: 0V

Place close
to Phase 1 L

Change size from 0603 to 0402.
Because no 0603 component can be used.

PHASE DETECTION

Place close
to Dr. MOS

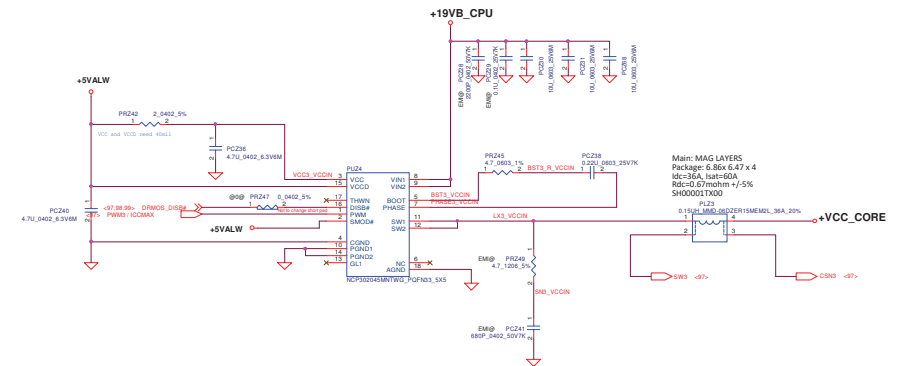
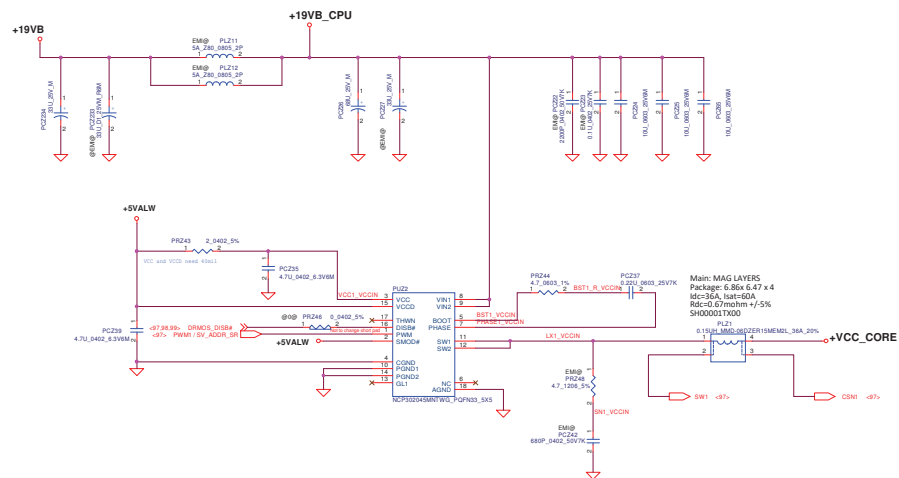
Place close
to Dr. MOS

Place close
to Phase 1 L

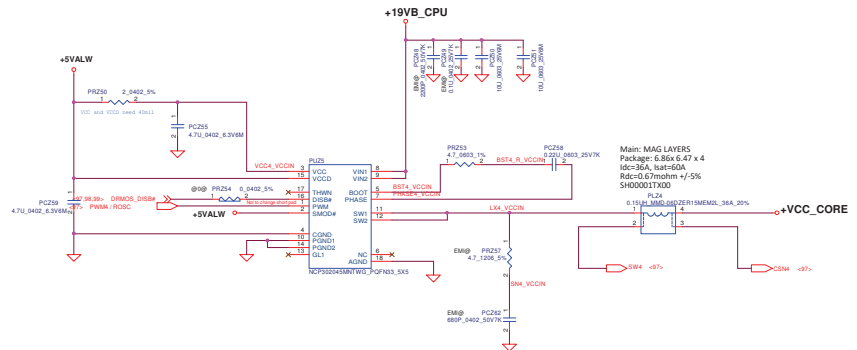
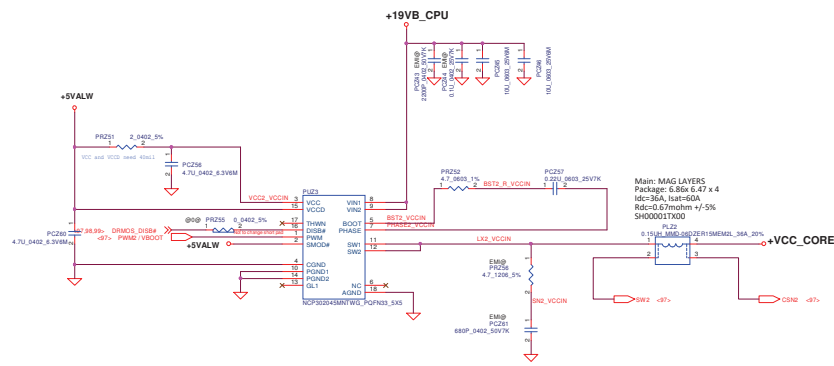
Place close
to Phase 1 L

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Issued Date	2020/03/05	Deciphered Date	2017/01/06	Title	+VCCORE
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Size	Document Number	HMS14 MB LA-1972P			
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Main Func = +VCC_CORE

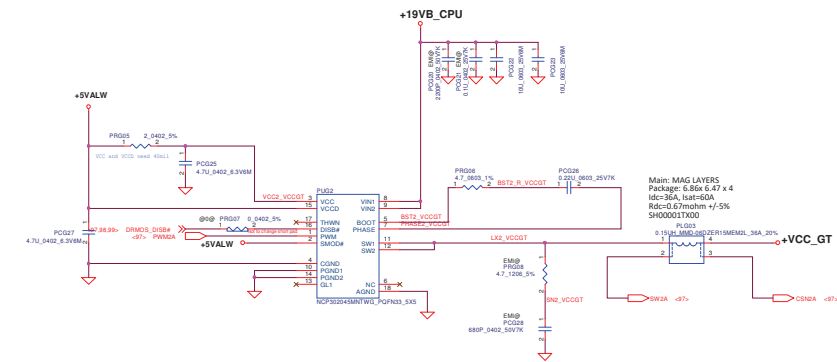
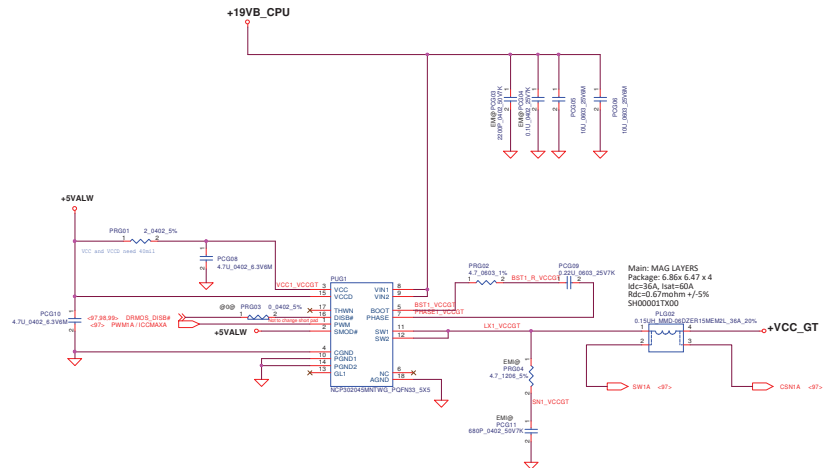


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					HS054 MSA 1A.1952P	16
				Date:	Wednesday, January 09, 2022	Page 38 of 121

Main Func = +VCC_GT

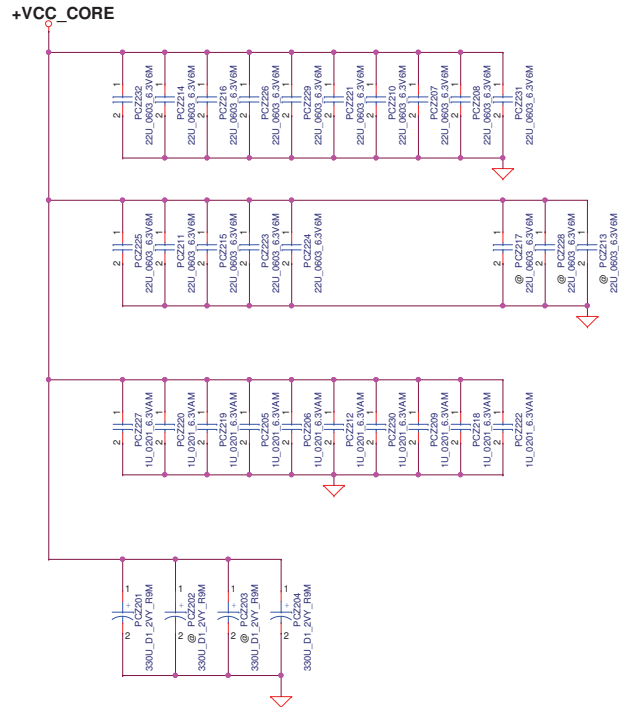


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Issued Date	2020/03/05	Declassified Date	2017/01/06	Title	+VCC_GT
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				Rev	1.0
				Date	Wednesday, January 05, 2020
				Sheet	69 of 121

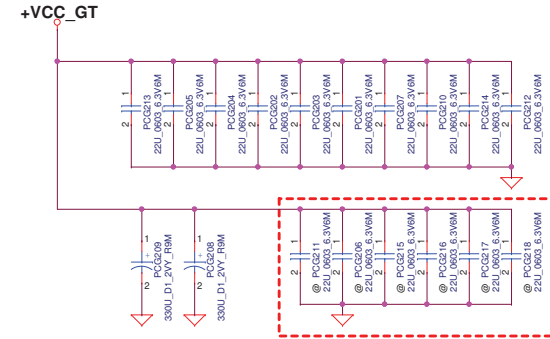
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+VCC_CORE Output CAP :  
330uF*4  
22uF_0603*15 (+3@)  
1uF_0201*10
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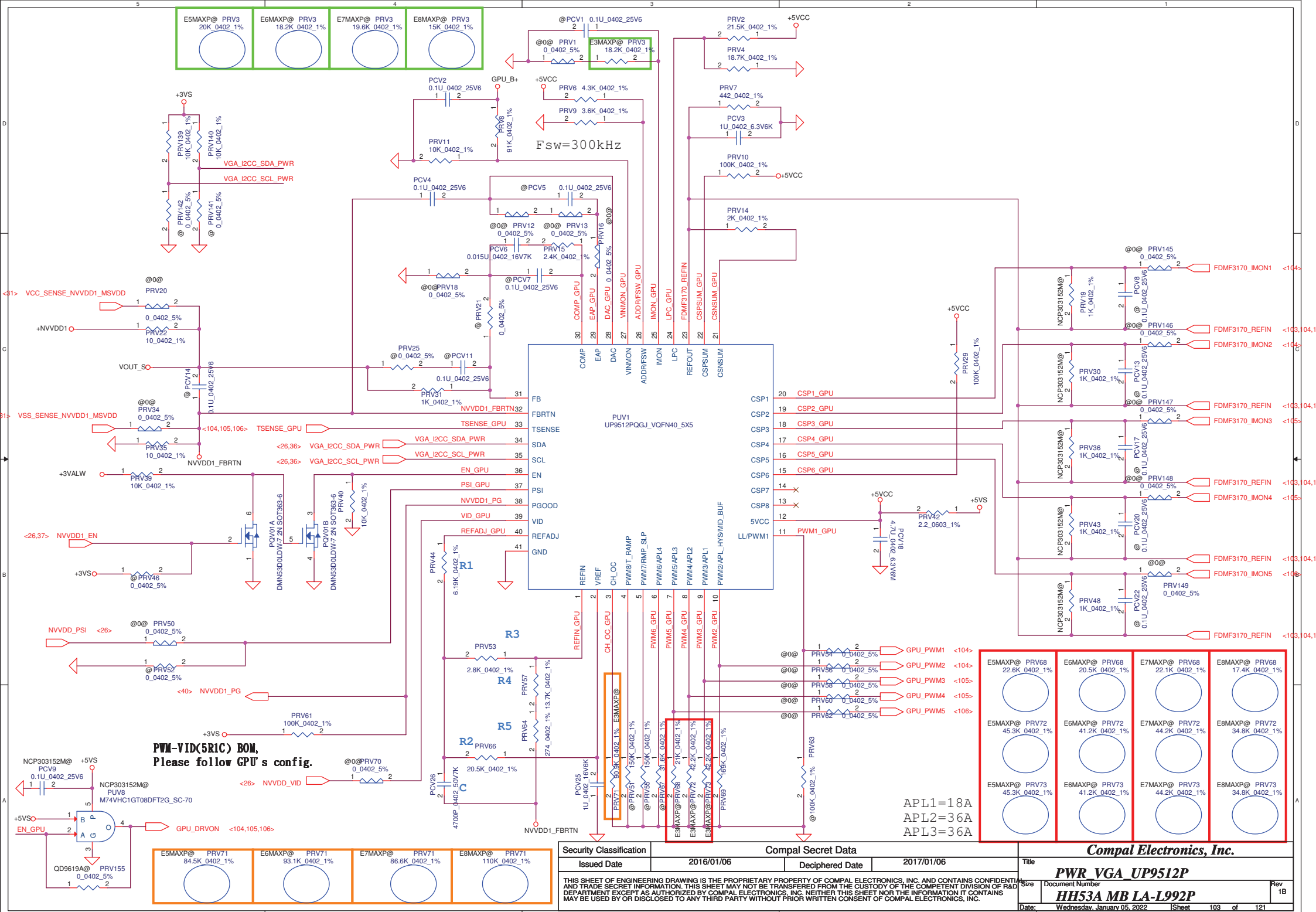
330uF*2
22uF_0603*10 (+6@)



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Issued Date	2020/02/27	Deciphered Date	2021/12/31	Title	PWR CPU Decoupling CAP
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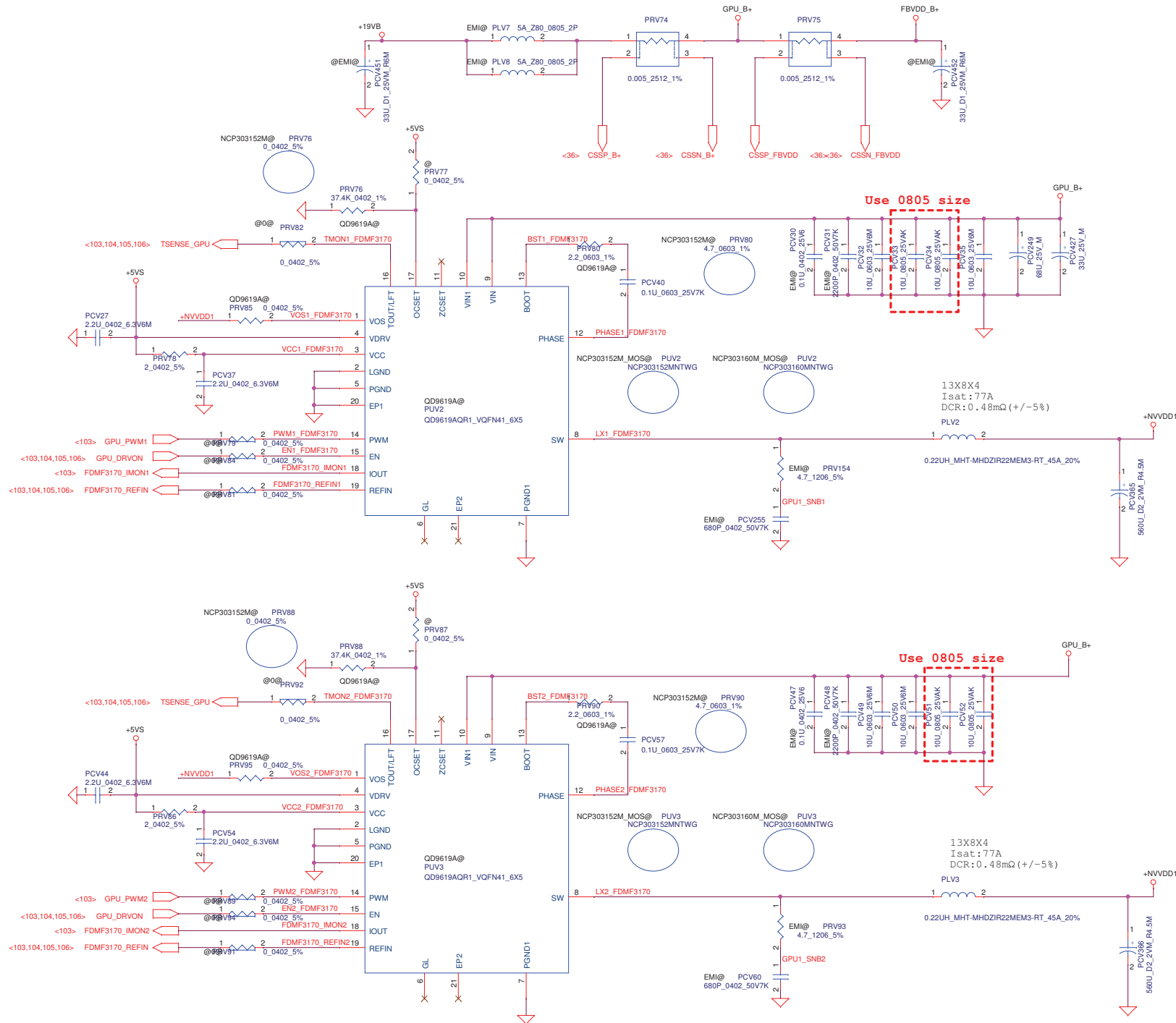
**PWM-VID(5R1C) BOM,
Please follow GPU's config.**

E5MAXP@ PRV71 84.5K 0402_1%	E6MAXP@ PRV71 93.1K 0402_1%	E7MAXP@ PRV71 86.6K 0402_1%	E8MAXP@ PRV71 110K 0402_1%
--------------------------------	--------------------------------	--------------------------------	-------------------------------

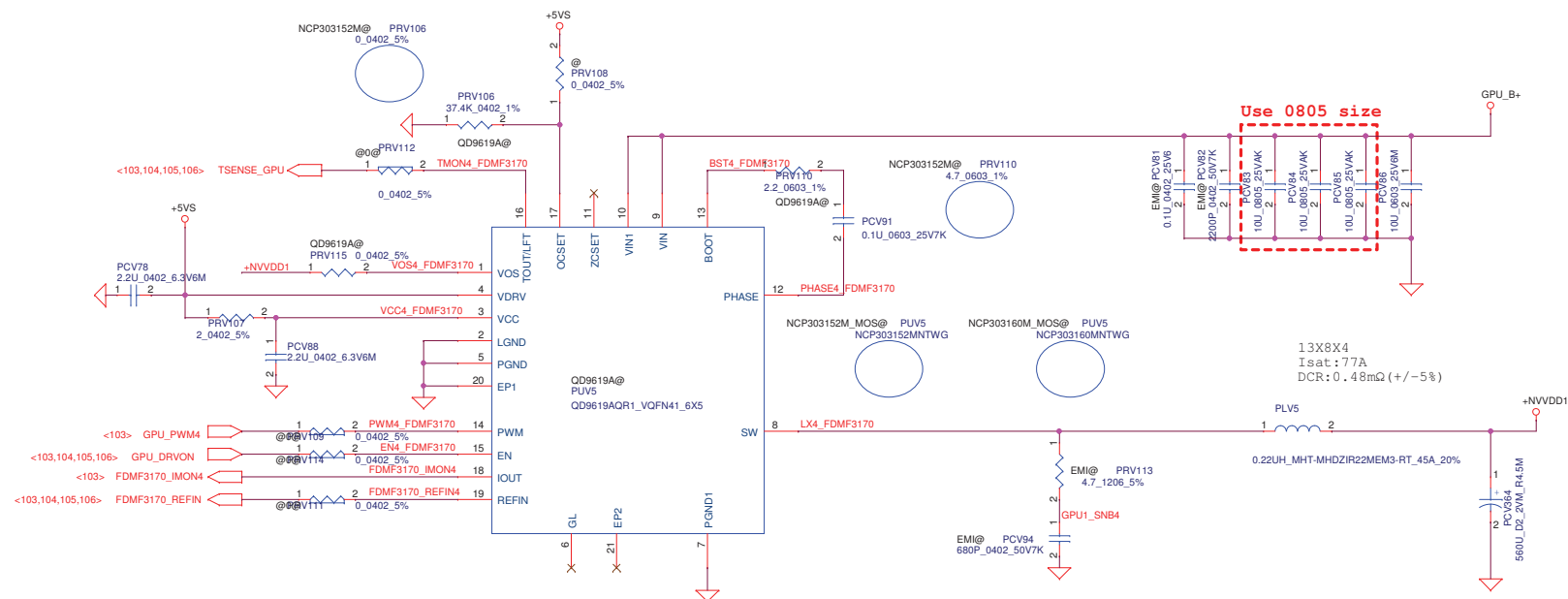
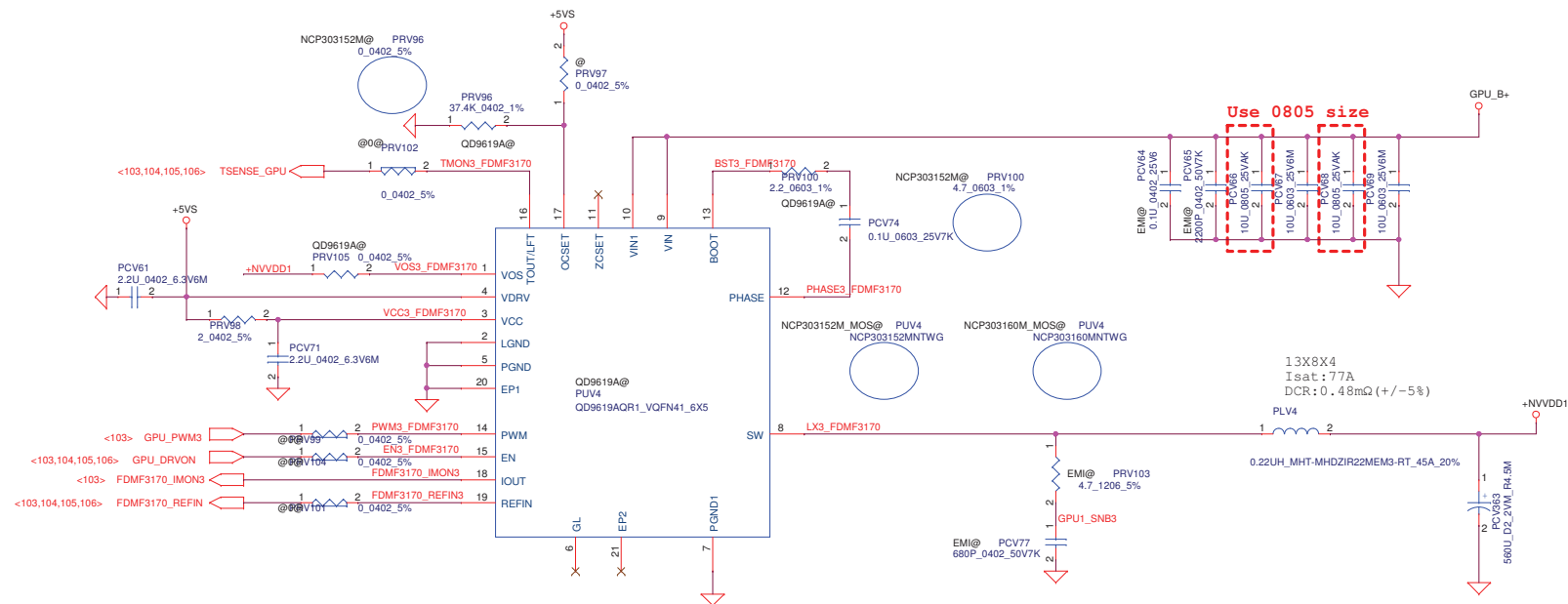
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E5MAXP@ PRV68 22.6K 0402_1%	E6MAXP@ PRV68 20.5K 0402_1%	E7MAXP@ PRV68 22.1K 0402_1%	E8MAXP@ PRV68 17.4K 0402_1%
E5MAXP@ PRV72 45.3K 0402_1%	E6MAXP@ PRV72 41.2K 0402_1%	E7MAXP@ PRV72 44.2K 0402_1%	E8MAXP@ PRV72 34.8K 0402_1%
E5MAXP@ PRV73 45.3K 0402_1%	E6MAXP@ PRV73 41.2K 0402_1%	E7MAXP@ PRV73 44.2K 0402_1%	E8MAXP@ PRV73 34.8K 0402_1%

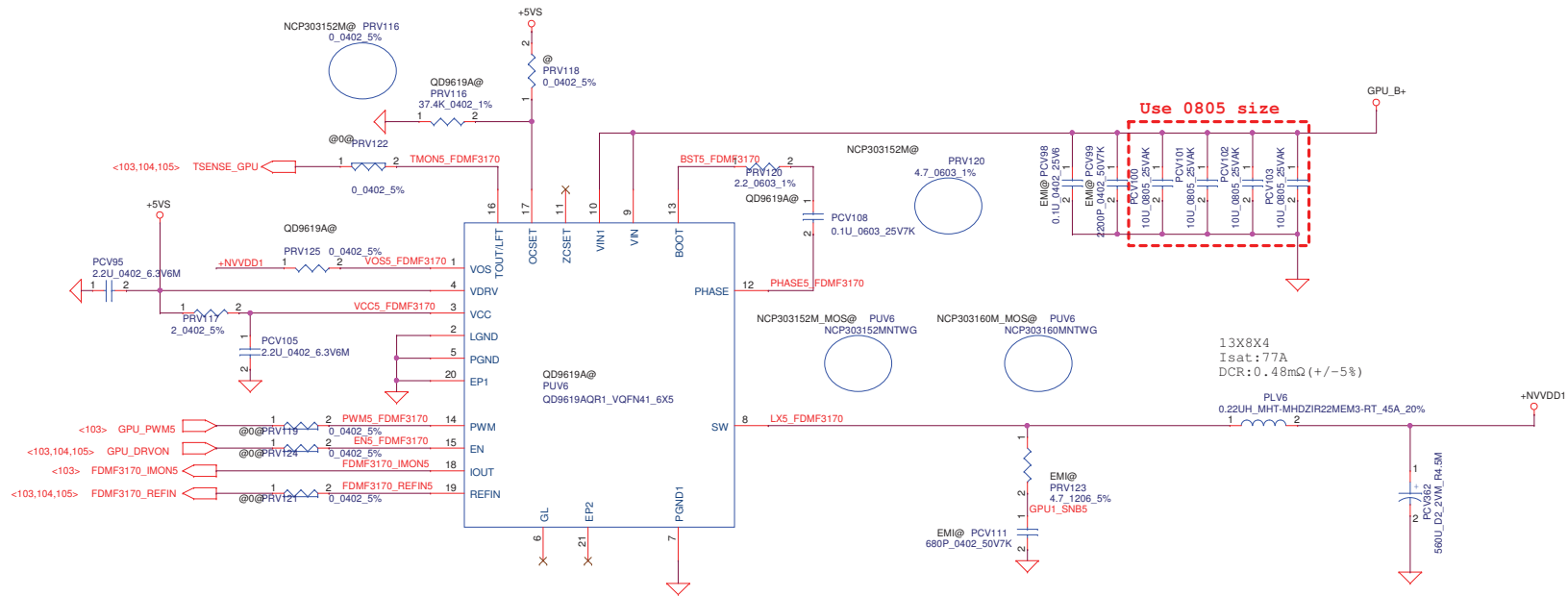
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PWR VGA UP9512P			
Size	Document Number	Rev	
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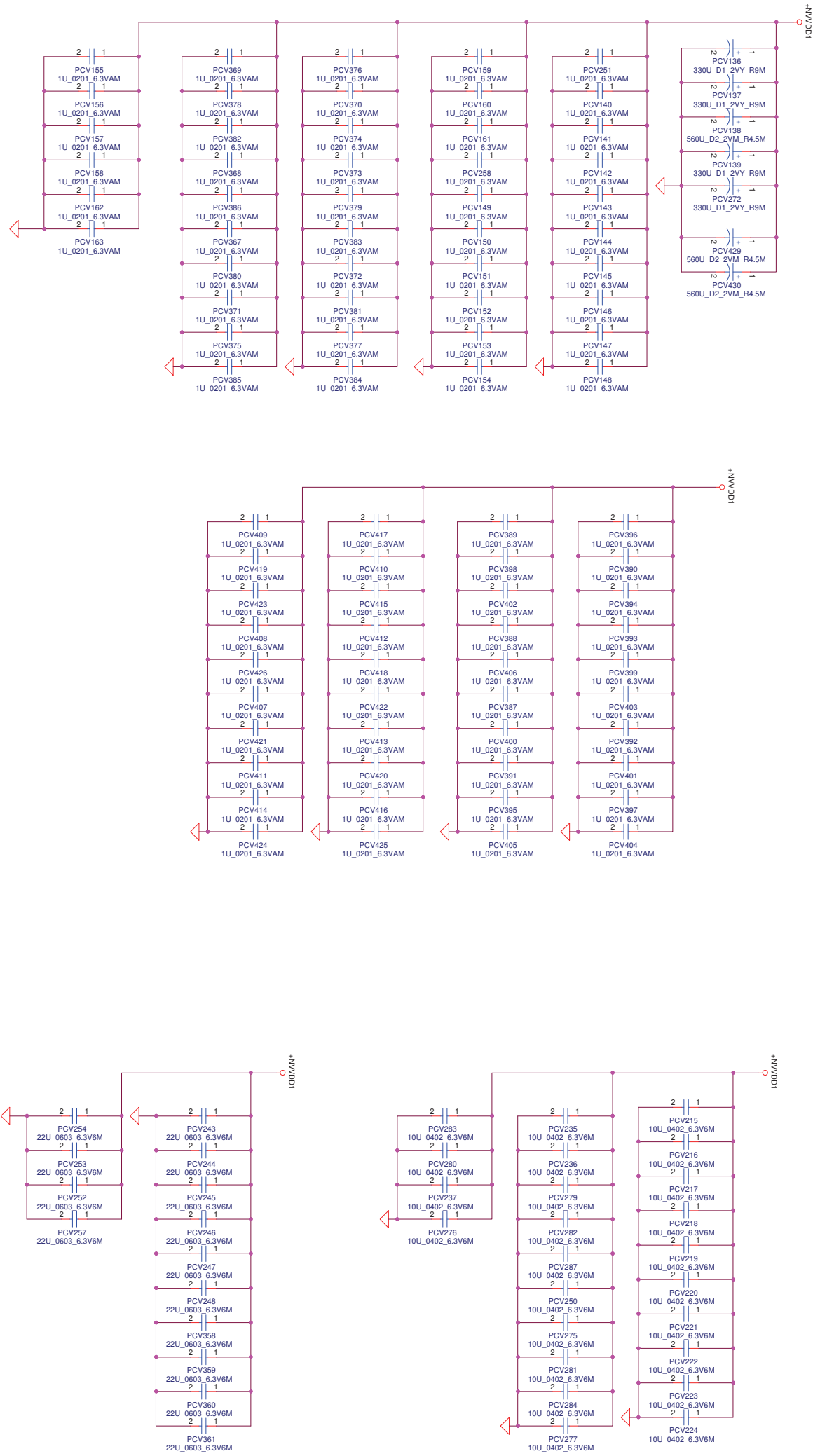
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Size	Document Number	Rev		1B	
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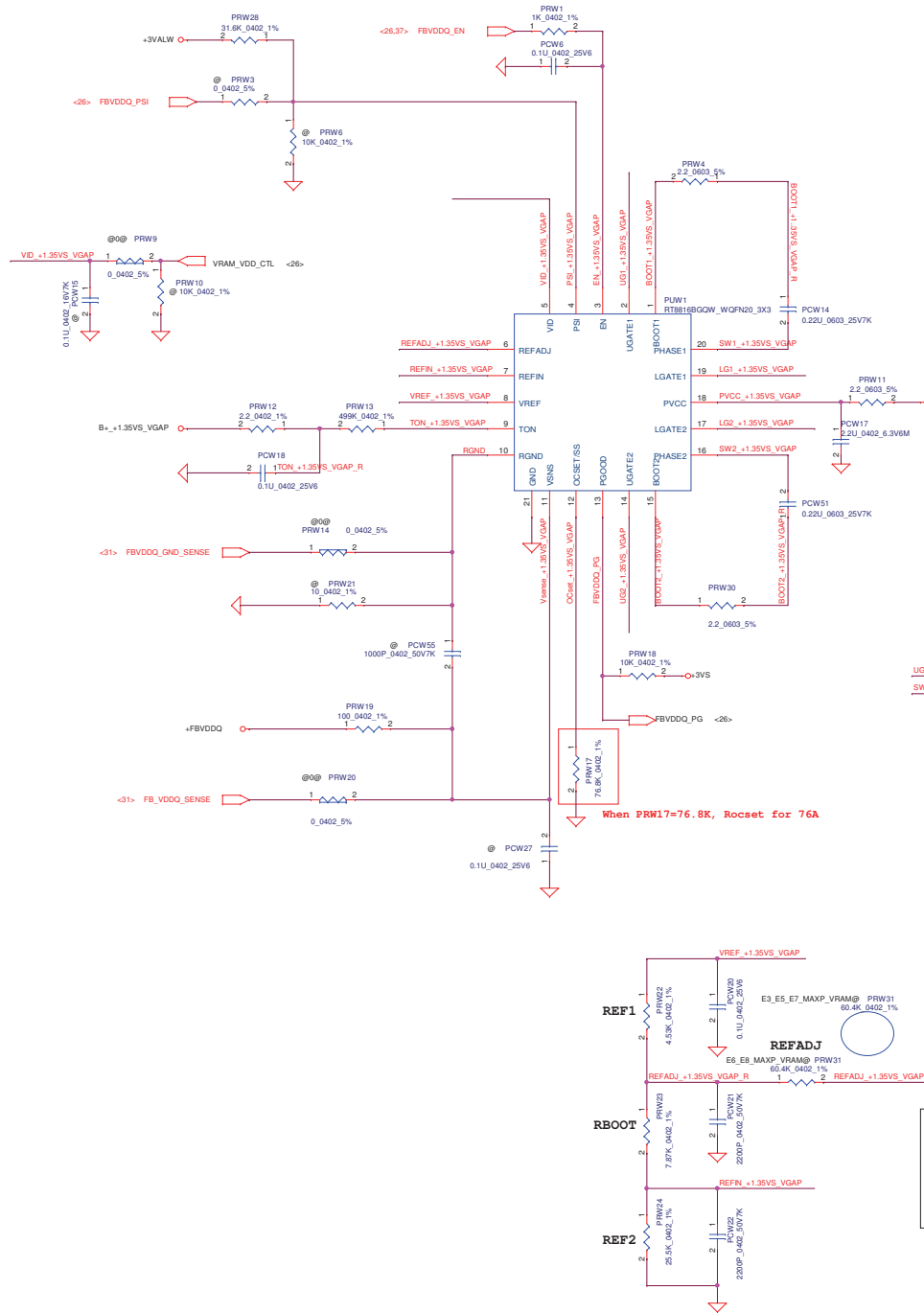
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR +NVVDDI		
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					HH514 MB LA-L972P	1B	
				Date:	Wednesday, January 05, 2022	Sheet	105 of 121



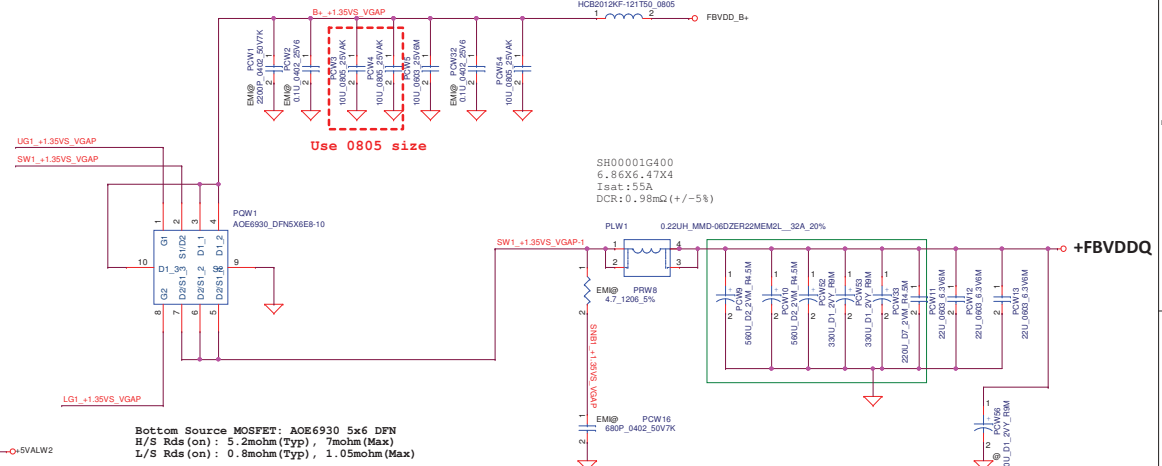
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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR +NVVDD1
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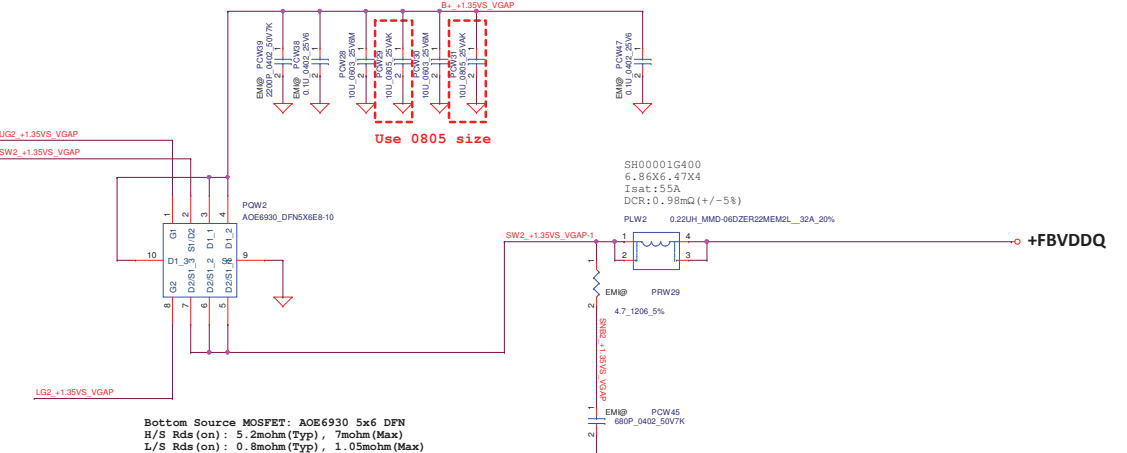
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108		107		121	



E6_E8_MAXP@
 E3_E5_E7_MAXP@
 When, VRAM_VDD_CTL=High
 Vboot=1.356V (x1.005)
 When, VRAM_VDD_CTL=Low
 Vboot=1.262V (x1.010)

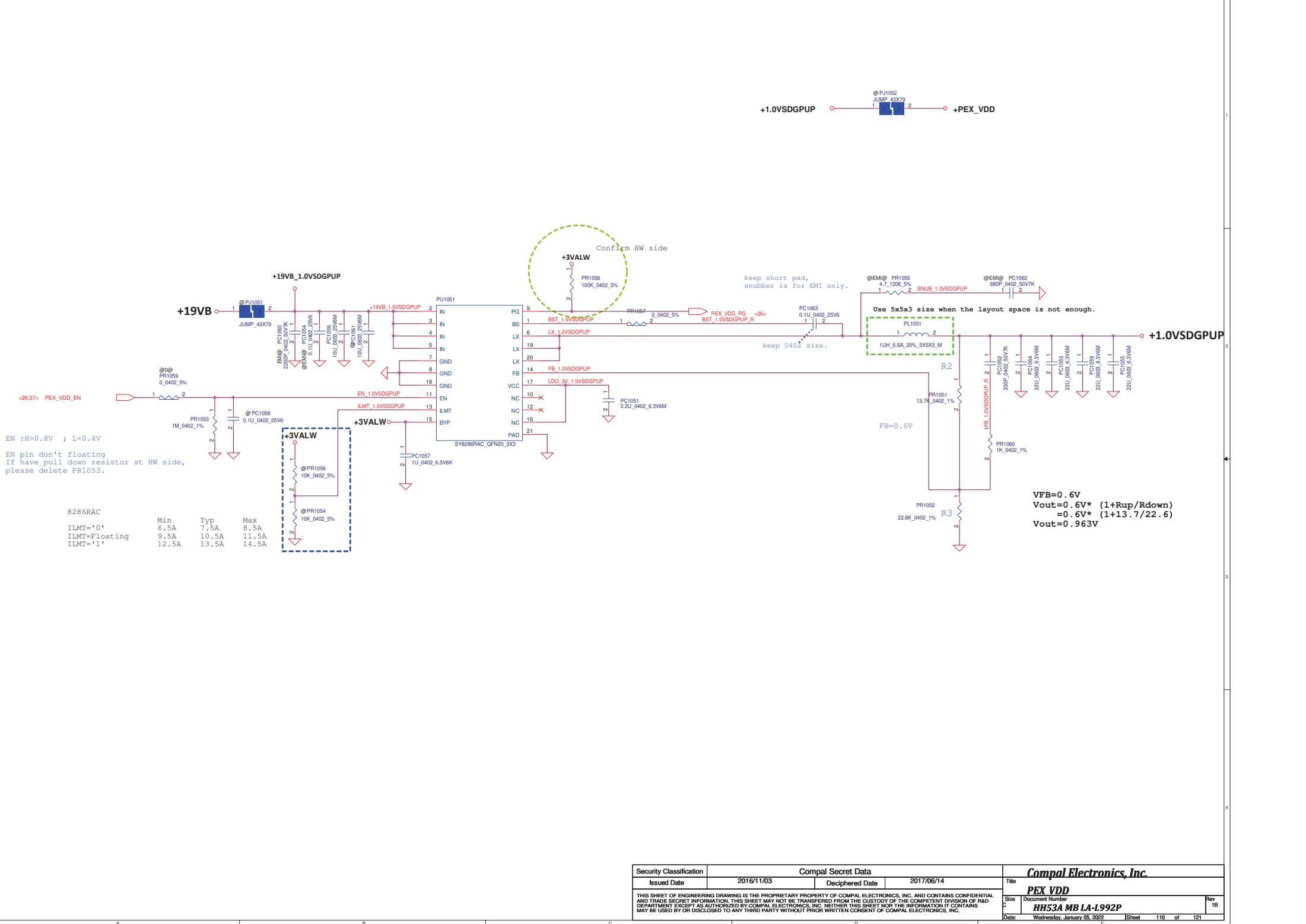


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EN :H>0.8V ; L<0.4V
EN pin don't floating
If have pull down resistor at HW side,
please delete PR1053.

8286RAC			
ILMT='0'	Min	Typ	Max
ILMT='0'	6.5A	7.5A	8.5A
ILMT='Floating'	9.5A	10.5A	11.5A
ILMT='1'	12.5A	13.5A	14.5A

$V_{FB}=0.6V$
 $V_{out}=0.6V * (1+R_{up}/R_{down})$
 $=0.6V * (1+13.7/22.6)$
 $V_{out}=0.963V$

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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	Reserve
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				Date: Wednesday, January 05, 2022	Sheet 112 of 121

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Item	Reason for change	PG#	Modify List	Date	Phase
01	Solution change	P.085	PQB22,PQB23,PQB24 (2N7002 SOT-323) change from SB000016E00 to SB000009Q80.	0729	DVT
02	PSYS modify	P.097	PRZ03 change from 20K_0402_1% (SD034200280) to 24.9K_0402_1% (SD034249280).	0804	DVT
03	Solution change	P.096, P.101	PCA201,PCA203,PCA204,PCA206,PCA207,PCA208,PCA209,PCA211,PCA212,PCA213,PCA216,PCA218,PCA220,PCA221,PCA222,PCA223,PCA225,PCA226,PCA227,PCA228,PCA202,PCA205,PCA210,PCA214,PCA215,PCA217,PCA219,PCA224,PCG201,PCG202,PCG203,PCG204,PCG205,PCG207,PCG210,PCG212,PCG213,PCG214,PCZ207,PCZ208,PCZ210,PCZ211,PCZ214,PCZ215,PCZ216,PCZ221,PCZ223,PCZ224,PCZ225,PCZ226,PCZ229,PCZ231,PCZ232 change from 22U_0603_6.3VAM (SE00001CA10) to 22U_0603_6.3V6M (SE00000M000).	0804	DVT
04	Solution change	P.085	PRB42 change from 0.01_2512_1% (SD00002A630) to 0.005_2512_1% (SD00001SZ00). PRB4 change from 0.01_2512_1% (SD00002A630) to un-pop. PRB37 connect net change from +19V_VIN to +19V_ADPIN_P1.	0811	DVT
05	12V_Fan fine turn	P.111	PR1205 change from 10K_0402_1% (SD034100280) to 56.2K_0402_1% (SD000001580). PC1209 change from 4700P_0402_25V (SE075472K80) to 330P_0402_50V (SE074331K80).	0811	DVT
06	Solution change	P.095, P.097 P.098, P.099	PCA03,PCA23,PCZ07 change from 2.2U_0402_6.3VAM (SE000011Z80) to 2.2U_0402_6.3V6M (SE000008880). PCA04 change from 0.22U_0402_25VAK (SE000013J00) to 0.22U_0402_25V6K (SE000015W00). PCZ55,PCZ59,PCG08,PCG10,PCG25,PCG27,PCZ35,PCZ36,PCZ39,PCZ40,PCZ56,PCZ60 change from 4.7U_0402_6.3VAM (SE00001BY00) to 4.7U_0402_6.3V6M (SE00000S000). PCA07,PCA30 change from 47U_0603_2.5VAM (SE00001FQ00) to 22U_0603_6.3V6M (SE00000M000). Add new location PCA51,PCA52 and pop 22U_0603_6.3V6M (SE00000M000).	0813	DVT
07	EMI Request	P.098, P104	PCZ27 change from pop to unpop Add new location PCZ233 and unpop 33U_25V Pos Cap(SGA0000A400) Add new location PCZ234 and pop 33U_25V OS Con (SF000007700) Add new location PCV451,PCV452 and unpop 33U_25V Pos Cap(SGA0000A400)	0830	DVT
08	CPU transient fine turn	P.095, P.097 P.101	PCA14 change from unpop to pop 3300P_0402_25V (SE075332K80). PUZ01 change PN from SA0000E6B10 (PC0) to SA0000E6B20 (PD0). PRZ18,PRZ20,PRZ14,PRZ74 change from 75K_0402_1% (SD034750280) to 140K_0402_1% (SD034140380) PCZ08,PCZ167 change from 390P_0402_50V (SE074391K80) to 270P_0402_50V (SE074271K80) PRZ77 change from 49.9K_0402_1% (SD034499280) to 24.3K_0402_1% (SD00000AT80) PRZ69,PRZ70 change from 47.5K_0603_1% (SD00000NN80) to 51.1K_0603_1% (SD014511280) PCZ202,PCZ203 change from pop 330U_D2_2V (SGA00009500) to unpop.	0830	DVT
09	Solution change	P.107	PCV429,PCV430 change from 220U_D7_2V (SGA0000AM00) to 560U_D2_2V (SGA00006J00). PCV136,PCV137 change from 560U_D2_2V (SGA00006J00) to 330U_D2_2V (SGA00009500).	0830	DVT
10	PD IC Solution change	P.083	Add new location PQ210, PQ212, and pop AONR21357 (SB00001MT00) Add new location PQ211 and pop 2N7002KW (SB000009Q80) Add new location PR220 and pop 49.9K_0402_1% (SD034499280) Add new location PR221 and pop 499K_0402_1% (SD034499380) Add new location PC203 and pop 2200P_0402_25V (SE075222K80)	0823	DVT
11	CIS symbol update	P.098, P.099	PUZ2, PUZ3, PUZ4, PUZ5, PUG1 and PUG2 update CIS symbol and re-link	0913	DVT
12	EMI Request	P.087, P.088 P.090, P.091	PR304,PR502,PR552,PR1106, PR1802 change from un-pop to pop 4.7_1206_5% (SD001470B80). PC314,PC513,PC563,PC1111, PC1806 change from un-pop to pop 680P_0402_50V (SE074681K80).	0917	DVT
13	CPU transient fine turn (GT prak 50A->55A)	P.097	PRZ103 change from 32.4K_0402_1% (SD034324280) to 33.2K_0402_1% (SD034332280). PRZ33 change from 49.9K_0402_1% (SD034499280) to 54.9K_0402_1% (SD00000H880). PRZ107 change from 21.5K_0402_1% (SD034215280) to 24.3K_0402_1% (SD00000AT80).	1001	DVT
14	Solution change	P.082, P.091 P.095, P.097 P.099, P.098 P.103, P.083 P.085, P.111 P.090, P.108	PR201 change from pop 0_0402_5% (SD028000080) to un-pop. PQ151 footprint change from "B5S138LT16_SOT23-3" to "LB5S139LT16_SOT23-3" PRA05,PRA13,PRA16,PRB16,PRZ10,PRZ21,PRZ22,PRZ30,PRZ41,PRZ98,PR1207,PR1208,PRG03,PRG07,PRZ46,PRZ47,PRZ54,PRZ55,PRB13,PRB17,PRB21,PRV1,PRV12,PR1811,PRV13,PRB51 change from pop 0_0402_5% (SD028000080) to R-short. (total 26 pcs) PR1105 change from 0_0402_5% (SD028000080) to 100K_0402_1% (SD034100380). PC1102 change from un-pop to pop 0.22U_0402_25V6K (SE000015W00). PRW25 rename PRW31 change from 36.5K_0402_1% (SD034365280) to 60.4K_0402_1% (SD034604280)	1012	PVT
15	Solution change	P.095	PRA03 PRA15 change from un-pop to pop 10K_0402_5% (SD034100280).	1116	PVT

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